Micro-Power Data Converters

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Outline

- Micro-power D/A converters:
    - Overview of CMOS DACs
    - Switched-capacitor DACs
    - Quasi-passive two-C DAC
    - Quasi-passive pipeline DAC
    - Delta-sigma DACs.

- Micro-power A/D converters:
    - Overview of CMOS ADCs
    - SAR ADC, pipeline SAR ADC
    - Multiplexed incremental ADC
    - Extended-count hybrid ADC.

Applications

- Battery-powered medical devices (hearing aids, ECG, EEG, etc. sensors, brain stimulators) ;

- Wireless sensor networks for industrial and environmental applications;

- RFID systems.

- Typical target specifications:

  DACs: BW up to 20 kHz, ENOB 14 - 15 bits, 20-bit input ;

  ADCs: BW = up to 5 kHz; ENOB > 12 bits; power < 5 microwatts; input signal amplitude 0.1 ~ 5 mV.

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Power Saving in Data Converters

- Stages: S/Hs, buffers, comparators, SC blocks.
- S/H: whenever possible, use passive (SC) circuitry; if not, use direct charge transfer (DCT) amplifier stage.
- Buffers: use DCT stage.
- Comparators: use dynamic circuitry.
- SC circuits: use minimally busy circuitry. Reduce dynamic power dissipation.
- Transistor circuits: consider weak inversion operation.
- Logic: consider asynchronous switching.

Classification of DACs

- "Nyquist-rate" DAC: memoryless, one-to-one correspondence between input digital word and output analog sample;

- "Oversampled" DAC: has memory (finite or infinite length), so digital output depends on all previous inputs and outputs.

- Sampling rates may not be very different.

Classification of Nyquist-rate DACs

Classification of Nyquist-rate D/A converters
(T=clock period, N=resolution in bits)

Algorithm	Conversion time	Latency (delay)	Resolution (typical)	Usual implementation
Parallel (flash)	T	T	5-12 bits	Current steering; voltage division; charge sharing
Pipeline	T	NT	8-12 bits	Passive SC; active (opamp) stages
Serial	NT	NT	8-12 bits	2-capacitor SC stage
Counting	$2^N T$	$2^N T$	15-22 bits	SC integrator + digital comparator

Nyquist-Rate DACs

- Parallel (flash) DACs: conversion time and latency is T; resolution $N < 10$ bits; implementation R-string or R-2R ladder, current sources, switched-capacitor (SC) stage.

- Pipelined DACs: conversion time T; latency NT; $N < 14$ bits; SC stages.

- Serial DACs: conversion time and latency NT; $N < 12$ bits; 2-C stages.

- Counting DAC: conversion time and latency = $2^N \cdot T$; $N < 24$ bits; SC or RC integrators.

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Oversampled CMOS DACs

- Nyquist-rate vs. oversampled DACs: in oversampled DAC, the word length can be reduced to 1 ~ 5 bits.

- Mismatch errors can be suppressed in signal band using dynamic element matching.

- High accuracy can be obtained with simple low-power analog circuitry, but complex digital delta-sigma loop and prefilter are required.

- May only be economical for high-resolution low-power DAC applications.

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Nyquist-Rate Parallel DACs

- R-string or R-2R ladder: large area, large mismatch errors, static dissipation – seldom practical in low-power applications.

- Current-source DAC: large mismatch error, static dissipation – seldom used in slow low-power DACs.

- SC stages: binary-weighted or unary (unit-element-based) charge redistribution circuits. Unary is more complex, but the glitches are reduced, the monotonicity is guaranteed, and dynamic element matching may be possible.
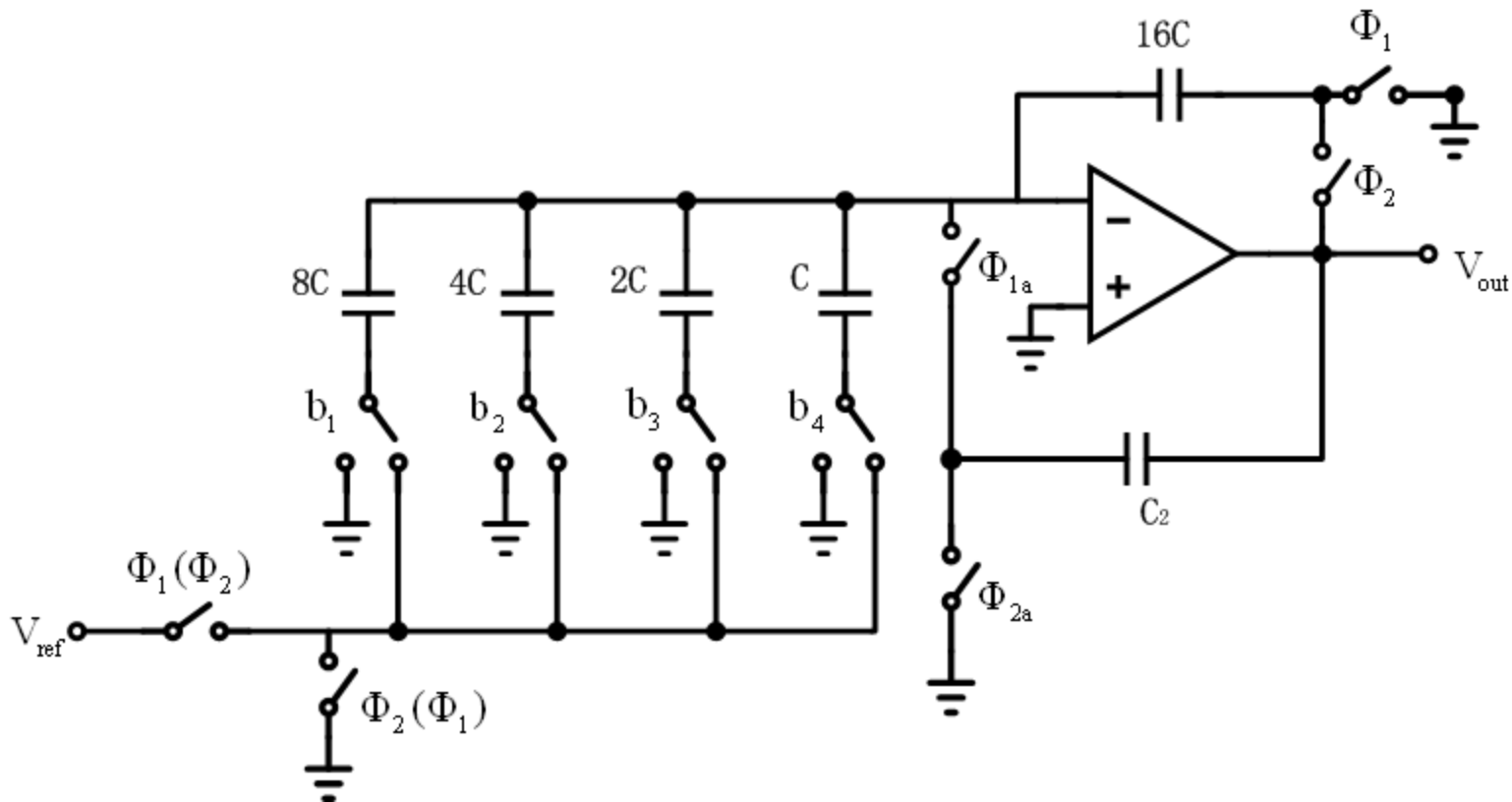
SC DAC Stages

- Unary SC DAC: monotonic, low glitch.
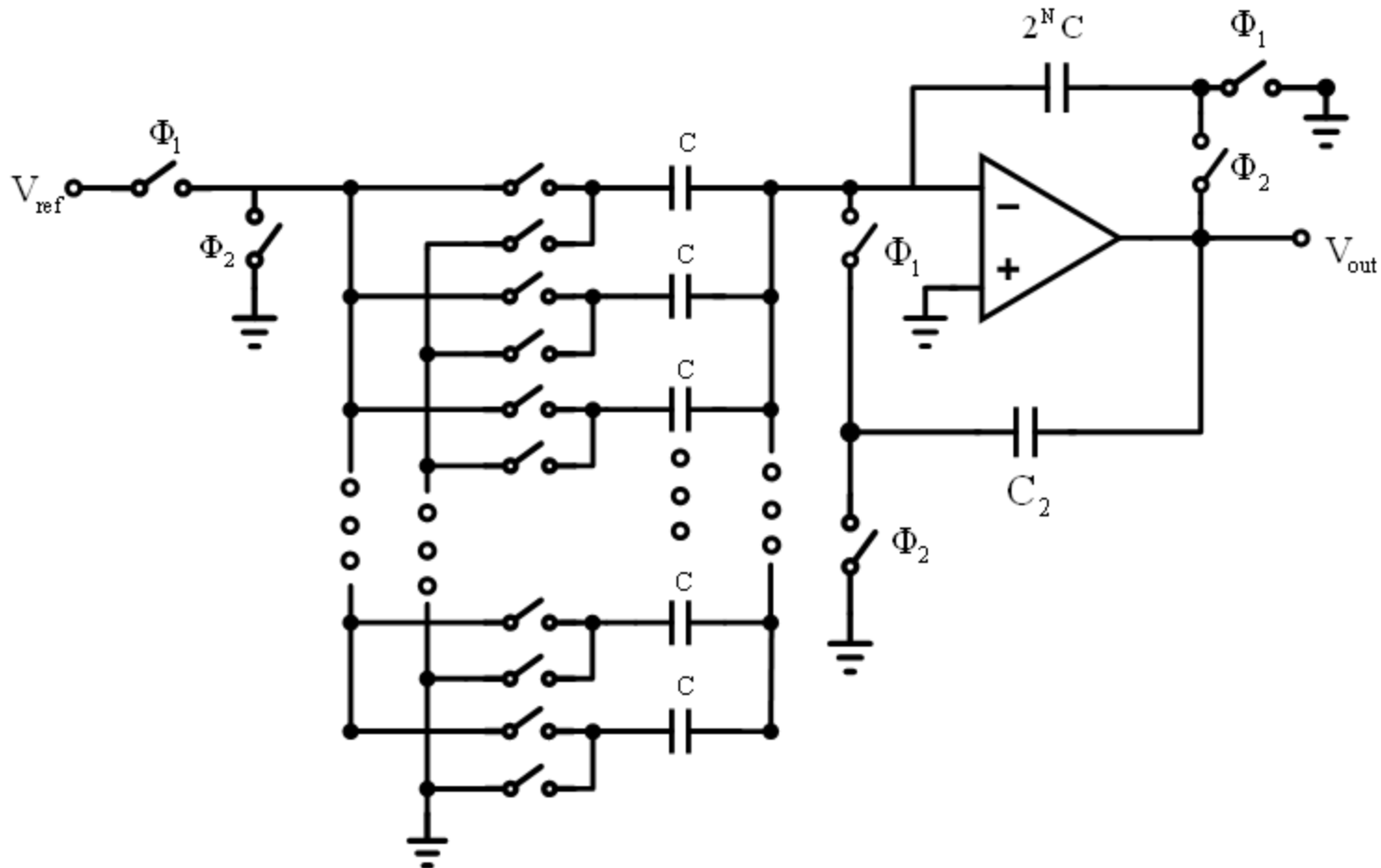
SC DAC Stages

- Binary SC DAC: non-monotonic, large glitch.

- Both circuits use correlated double sampling for amplifier offset cancellation and for gain boosting.

SC DAC Using DCT Circuit

- Direct charge transfer (DCT) reduces the slewing and settling requirements on the amplifier, since it need not provide current to the feedback branch:

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Two-Capacitor DAC

- Simple and fast, but mismatch introduces large spurs.
- Digital dither, correction or mismatch shaping possible.
- Serial DAC; needs N clock periods for N-bit resolution.
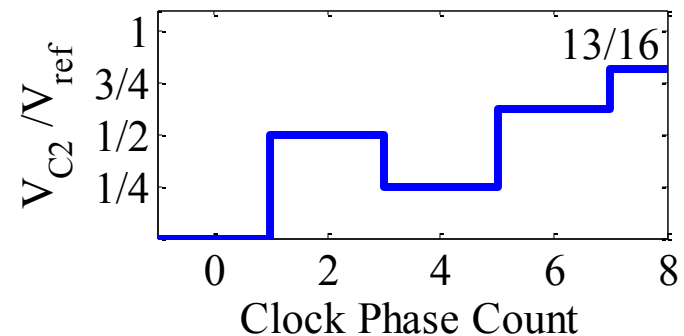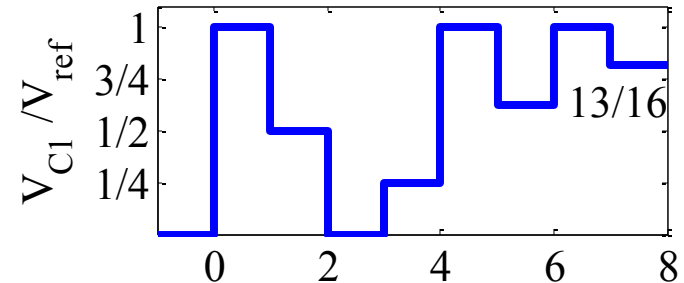- May be time interleaved for Nyquist-rate operation.
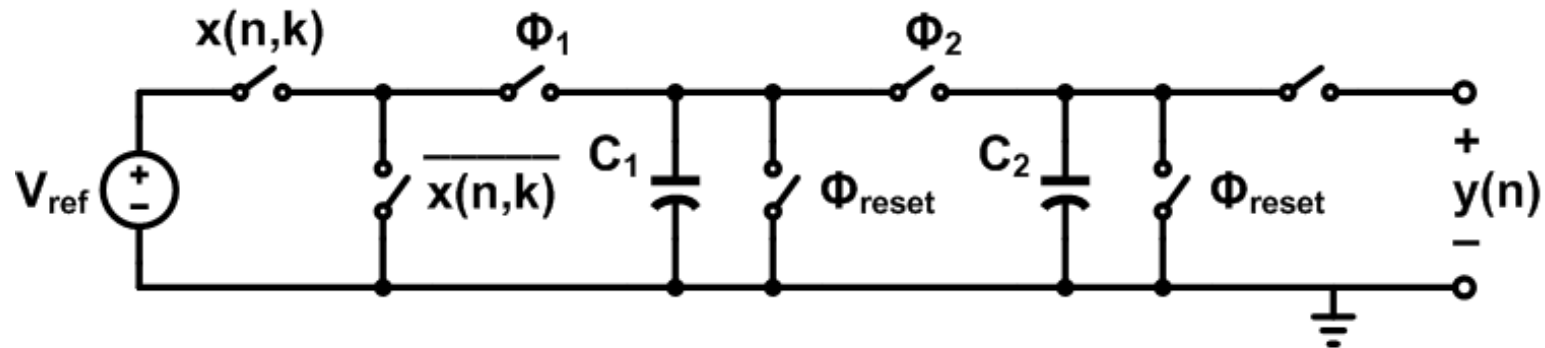
Quasi-Passive Cyclic DAC

- ## Operation for x(n) = 1, 0, 1, 1:

  - Charge redistribution between two equal-valued capacitors
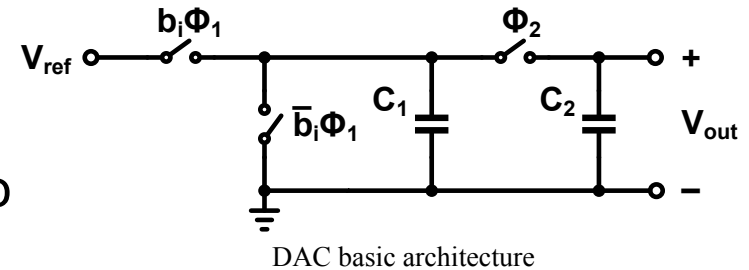
  - Serial digital input; LSB first

  - Φ_1 and Φ_2 are two non-overlapping clock phases

  - Conversion follows equation

$$V_{out} = V_{ref} \sum_{i=1}^{N} b_i 2^{-i}$$
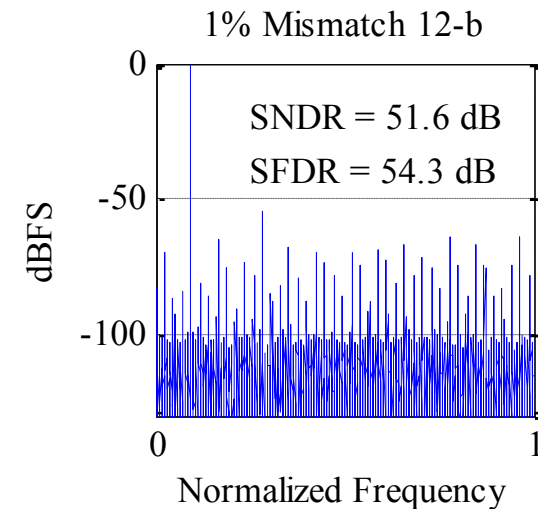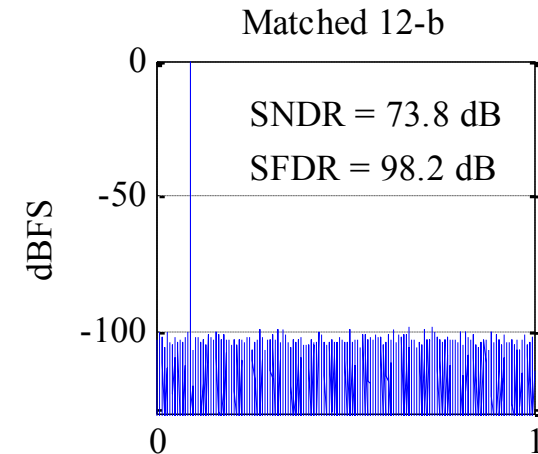

DAC basic architecture

Conversion sequence for input '1101'

[1] R. E. Suarez et al., "All-MOS charge distribution analog-to-digital conversion techniques – Part II," *JSSC*, Dec. 1975, pp. 379-385.

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Capacitor Mismatch

- Capacitor mismatch effects

  – Conversion accuracy limited
  by capacitor matching
  accuracy;

  – Capacitor mismatch
  introduces nonlinearity;

  – Plots show performance
  degradation (bottom) in SNDR
  and SFDR compared with
  output spectrum from DAC
  with ideal matching (top)

Matched 12-b

SNDR = 73.8 dB
SFDR = 98.2 dB

1% Mismatch 12-b

SNDR = 51.6 dB
SFDR = 54.3 dB

Normalized Frequency

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Mismatch Compensation (1)

- ## Switching techniques:
  - – Compensative switching
    - The roles of the two capacitor is interchangeable
    - The roles of the capacitors can be chosen for every bit
    - An algorithm was developed to minimize the conversion error for any digital word
    - The switching pattern is input dependent
    - First-order error canceled for 31% of the input codes; reduced to 1/10 for 48% of the input codes.
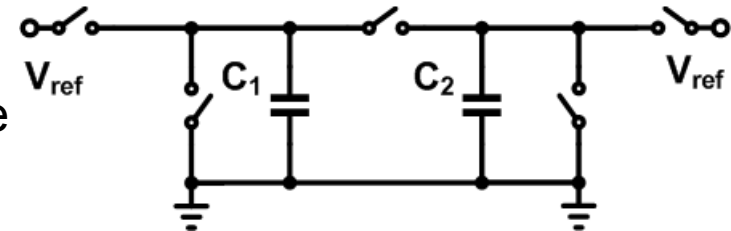
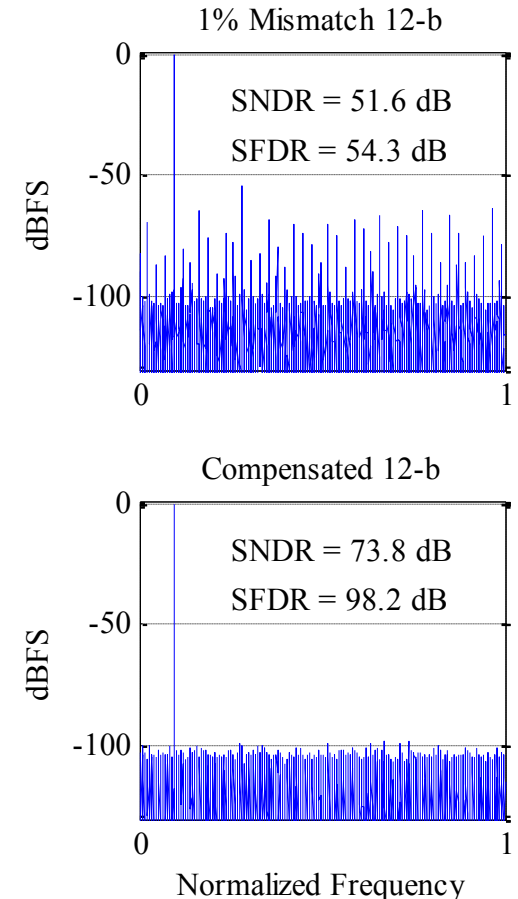The roles of the two capacitors are interchangeable with additional switches

[2] Weyten, L.; Audenaert, S., "Two-capacitor DAC with compensative switching," *Electronics Letters* , vol.31, no.17, pp. 1435-1437, 17 Aug 1995.

Mismatch Compensation (2)

- Switching techniques:

  - Complementary switching:

    - Digital word fed to DAC twice; once with normal arrangement, once with swapped roles of C_1 and C_2

    - Outputs of the two conversions are added (or averaged), actively or passively;

    - First-order mismatch compensation, at cost of doubled conversion time.

[3] Rombouts, P.; Weyten, L., "Linearity improvement for the switched-capacitor DAC," *Electronics Letters* , vol.32, no.4, pp.293-294, 15 Feb 1996.

1% Mismatch 12-b

SNDR = 51.6 dB
SFDR = 54.3 dB

dBFS

Compensated 12-b

SNDR = 73.8 dB
SFDR = 98.2 dB

dBFS

Normalized Frequency

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Mismatch Compensation (3)

- ## Switching techniques:
  - ### Input-word-splitting compensative switching
    - Compensative switching [2] does not compensate for all input codes
    - Split digital input into sum of two digital codes
    - The conversion errors reduced using compensative switching for the two new digital inputs
    - Final output is the sum of the two conversions

    - Needs two sets of 2-C DACs
    - Needs analog summation
    - Needs sophisticated algorithm for splitting the input word

[4] Rombouts, P.; Weyten, L.; Raman, J.; Audenaert, S., "Capacitor mismatch compensation for the quasi-passive-switched-capacitor DAC," *Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on* , vol. 45, no.1, pp.68-71, Jan 1998.

Mismatch Compensation (4)

- Switching techniques

  - Alternately complementary switching
    - Roles of C_1 and C_2 are swapped alternately in the first cycle and adopt complementary switching [3] for the second conversion cycle
    - Output of the two conversions are summed (or averaged)
    - INL improved due to cancellation of major second-order error

  - Hybrid switching
    - Averaging conversion results of complementary switching and alternately complementary switching
    - Smaller INL; fourfold conversion cycles

[5] Poki Chen; Ting-Chun Liu, "Switching Schemes for Reducing Capacitor Mismatch Sensitivity of Quasi-Passive Cyclic DAC," *Circuits and Systems II: Express Briefs, IEEE Transactions on* , vol.56, no.1, pp.26-30, Jan. 2009
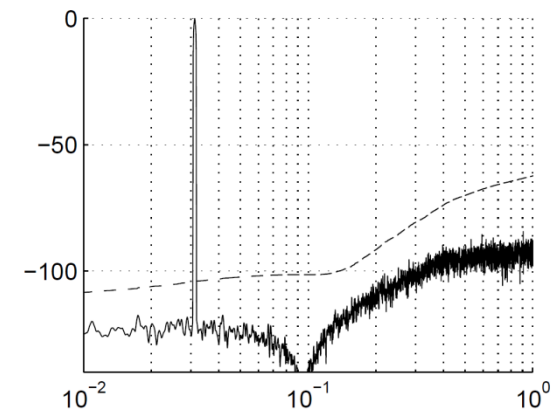
Mismatch Compensation (5)

- ## Mismatch shaping

  - ### Using oversampling ΔΣ Modulator

    - Digital state machine to control switching sequence of a symmetric two-capacitor DAC

    - Improved linearity; better shaping for higher OSR

    - Needs 2N clock cycles for N-bit D/A

[6] Steensgaard, J.; Moon, U.-K.; Temes, G.C., "Mismatch-shaping serial digital-to-analog converter," *Circuits and Systems, 1999. ISCAS '99. Proceedings of the 1999 IEEE International Symposium on* , vol.2, no., pp.5-8 vol.2, Jul 1999
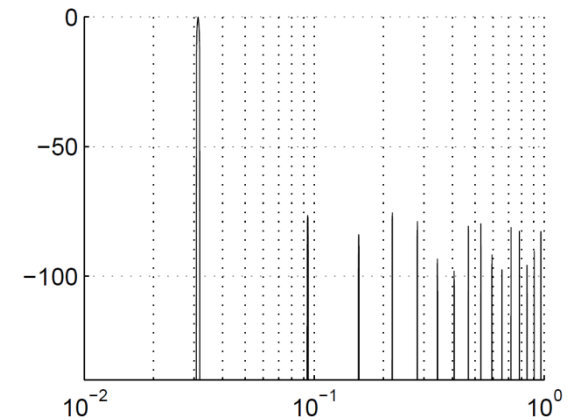
(a) dB vs. $2f/f_s$

(b) dB vs. $2f/f_s$

Simulated (FFT) performance of the DAC without (a) and with (b) mismatch shaping using a second-order loop filter

Mismatch Compensation (6)

- ## Radix-Based Digital Correction
  - ### Compensation in digital domain
    - Effectively a radix-(C_1/C_2) conversion
      $$V_{out} = V_{ref}(C_1/C_2)\sum_{i=1}^{N} b_i \left(1 + C_1/C_2\right)^{-1}$$
    - Assumes known mismatch $2(C_1-C_2)/(C_1+C_2)$, or C_1/C_2
    - ADC-like algorithm predistorts digital input
    - Feeds predistorted digital words into the 2-C DAC
    - Better performance when DAC resolution is high
    - Needs value of mismatch, with high accuracy.
   - J. Cao et al., ISCAS 2010
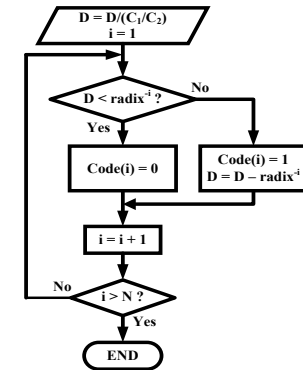
Radix-based digital pre-distortion algorithm flowchart
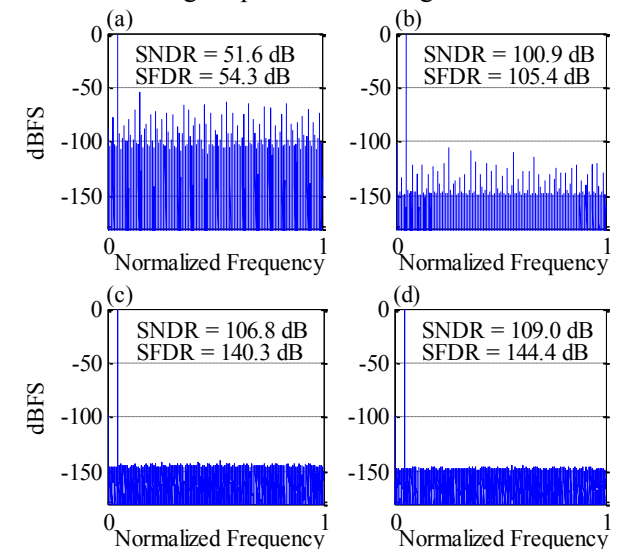
DAC output spectra plots for (a) uncompensated condition, (b) alternately complementary switching, (c) radix-based algorithm and (d) radix-based algorithm with one extra bit.

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Two-Capacitor DAC Variations

- ## Time interleaved 2-C DAC
  - Time interleaving 2-C blocks improves throughput speed
  - Capacitor mismatch *between* channels is tolerable
  - Direct-charge-transfer buffer reduces power consumption

- ## Pipelined quasi-passive cyclic DAC
  - Same operation as 2-C DAC
 - Information passed on to the last capacitor and DCT output buffer
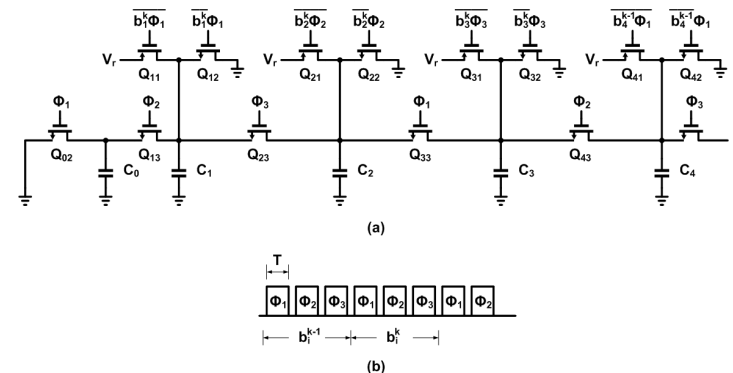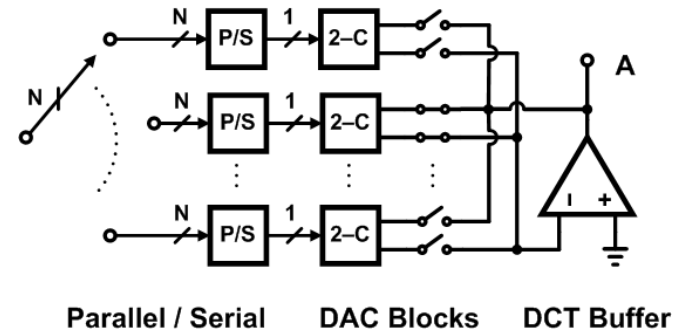
[7] Wang, F.-J.; Temes, G.C.; Law, S., "A quasi-passive CMOS pipeline D/A converter," *Solid-State Circuits, IEEE Journal of* , vol.24, no.6, pp. 1752-1755, Dec 1989

Quasi-Passive SC Pipeline DAC

- Serial digital input, Nyquist-rate output;
- Tolerant to switch nonidealities; little glitching
- Capacitor mismatches, DCT buffer errors limit operation to 11 – 12 bit accuracy.
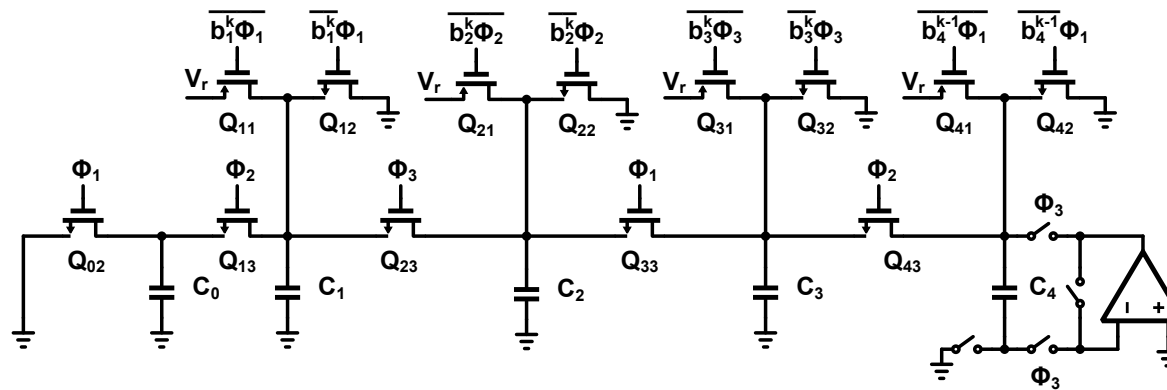

(a)
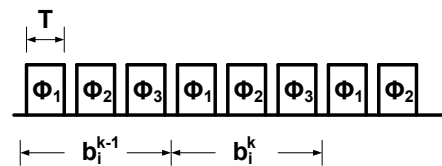
(b)

SC Pipeline DAC

Operation:

- Pipelined version of the two-C DAC.

- Bits are entered serially, starting with LSB controlling the charging of C_1.

- Charges are shared between adjacent capacitors, rippling down the pipeline.

- After delivering charge, each C is free to receive new one.

- Three clock phases needed.

- Last C voltage is buffered and read out.

Segmented SC Pipeline DAC

- For high accuracy, the pipeline DAC may be combined with a unary MSB DAC, and use dynamic element matching (DEM).

- Unary DAC with DCT buffer:
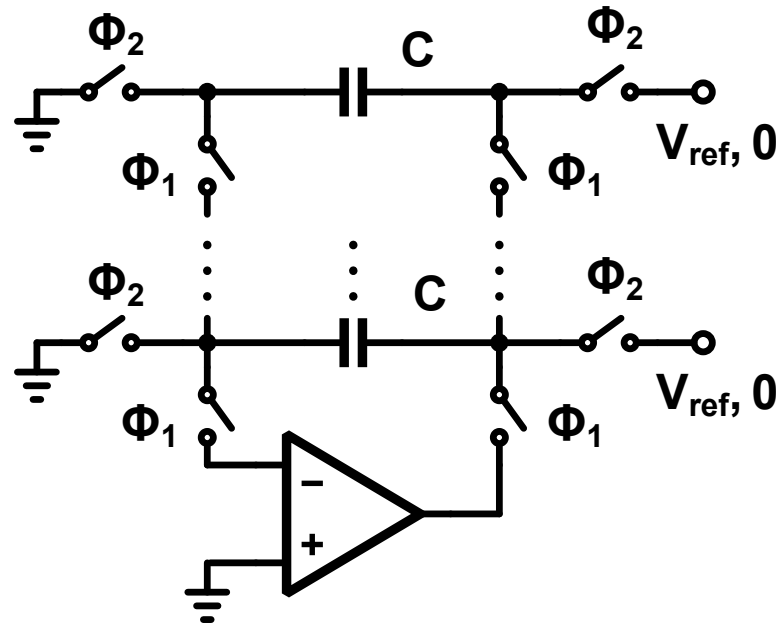
Quasi-Passive Pipeline DAC Schematic

- Operates from LSB toward MSB
- Pipelined operation by 3-bit segments of each input digital word
- Charges are shared by adjacent capacitors
- For *N*-bit conversion, it requires *N+1* equal valued capacitors
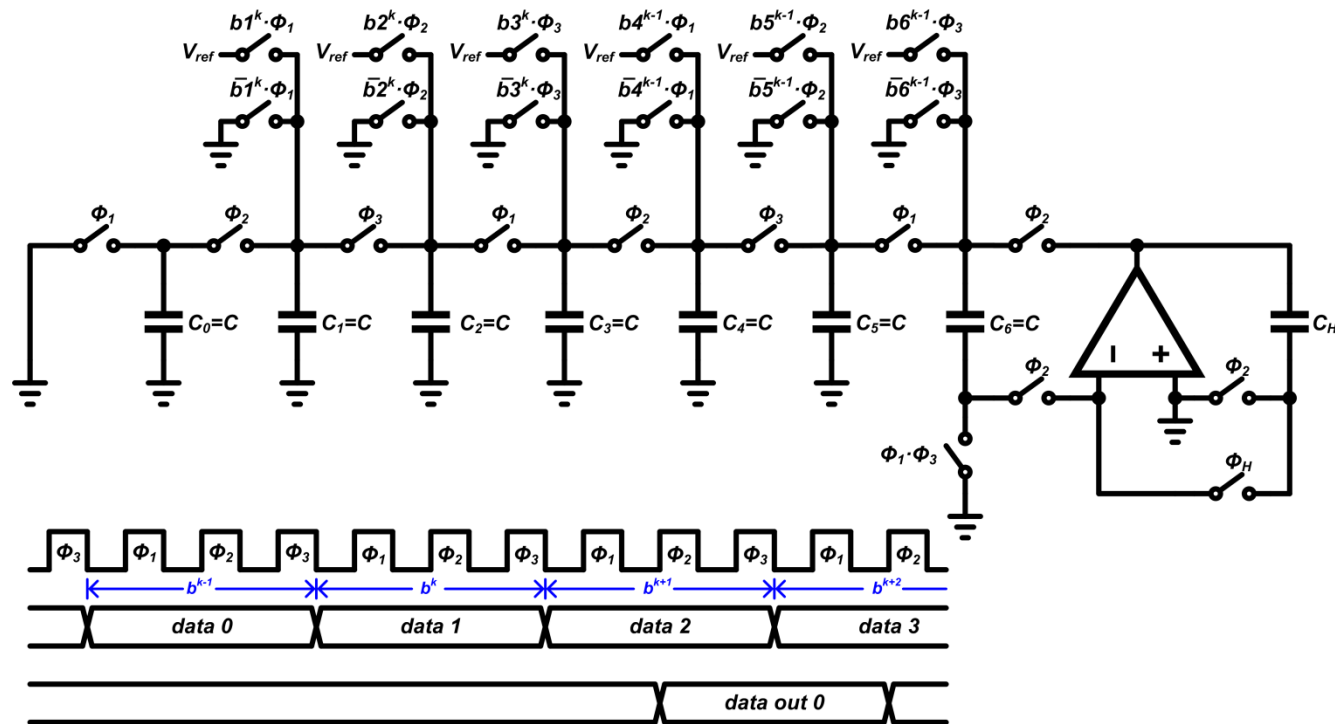
Wang, F.-J.; Temes, G.C.; Law, S., "A quasi-passive CMOS pipeline D/A converter," *Solid-State Circuits, IEEE Journal of* , vol.24, no.6, pp.1752-1755, Dec 1989

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Segmented DAC Realization

- Example of 6-bit DAC with 4+2 segmentation.

- For N bits, it requires $(n_{LSB}+1)+(2^{n_{MSB}}-1)$ equal valued capacitors, where $N = n_{LSB} + n_{MSB}$.
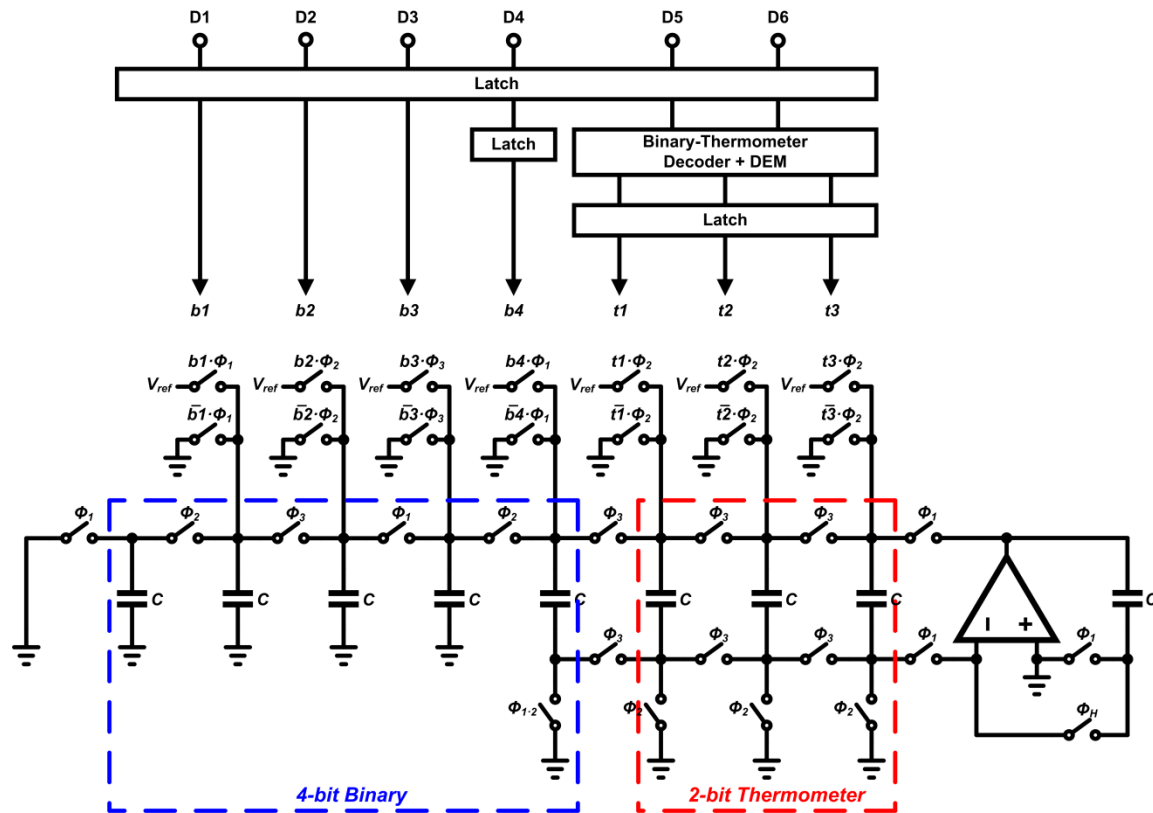
Multi-Segmented DAC Realization

- Example of 6-bit DAC with 2+2+2 segmentation
- For N bits, it requires $(n_{LSB}+1)C + (2^{n_{intermediate}} - 1)C + (2^{n_{MSB}} - 1)(2^{n_{intermediate}} C)$
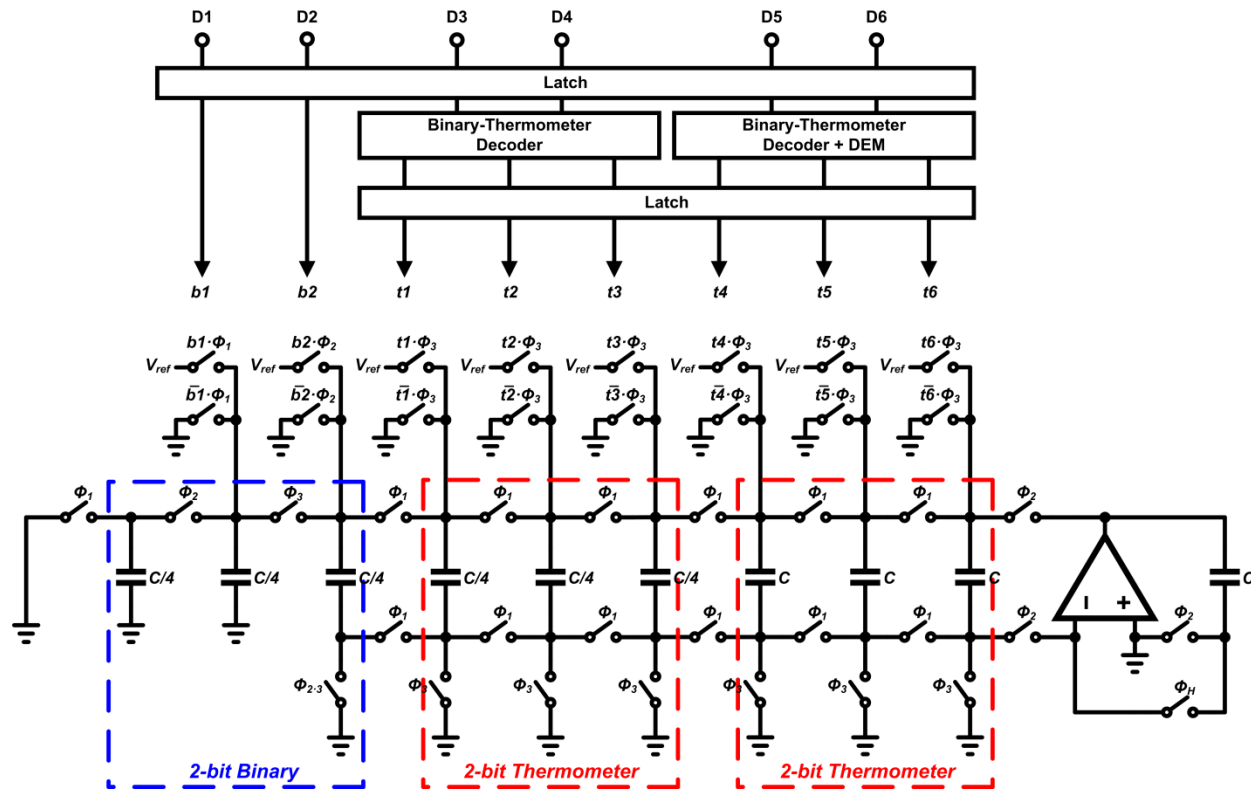 where $N = n_{LSB} + n_{intermediate} + n_{MSB}$

Fig. 6-bit DAC realization

Dynamic Element Matching (DEM)

- Multi-Segmented Quasi-Passive Pipeline DAC (7+4+4). 0.1% error.
- Response on the left is without DWA, and on the right is with DWA.

Fig. DWA Effect

ΔΣ DAC Structure

IF: Interpolation Filter
NL: Noise-shaping Loop
DAC: Digital-Analog Converter
LPF: Lowpass Filter
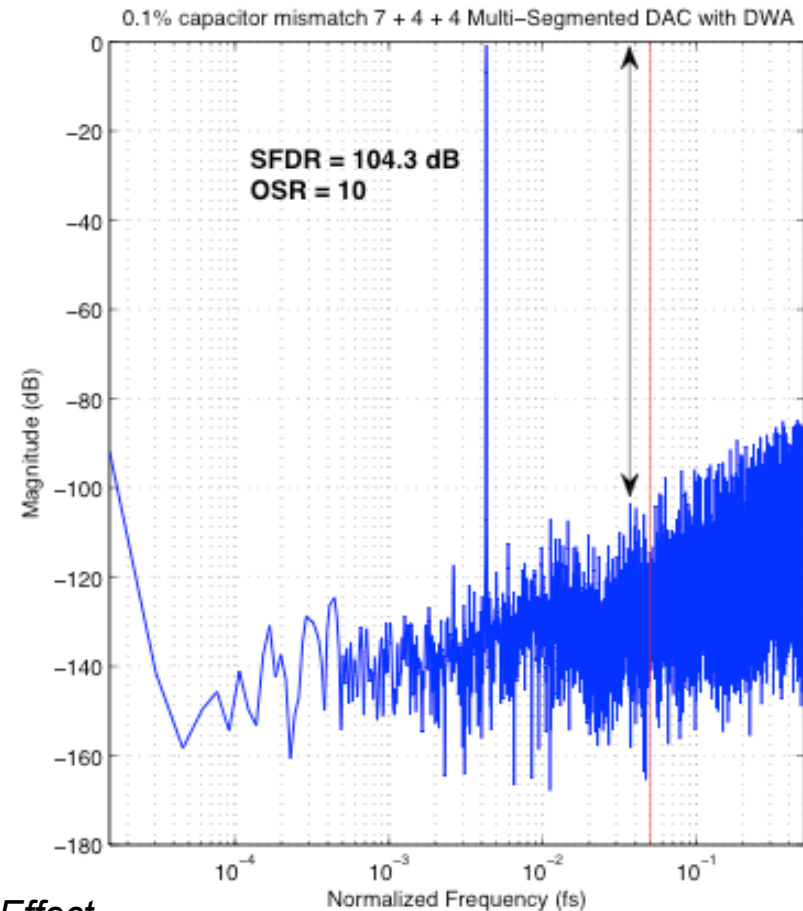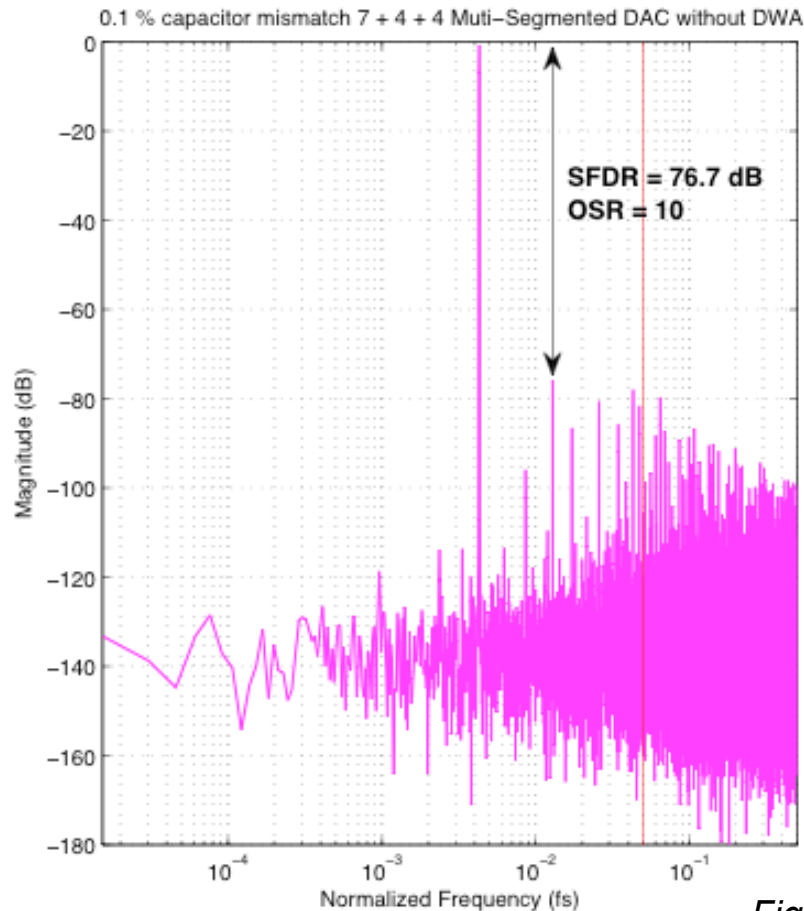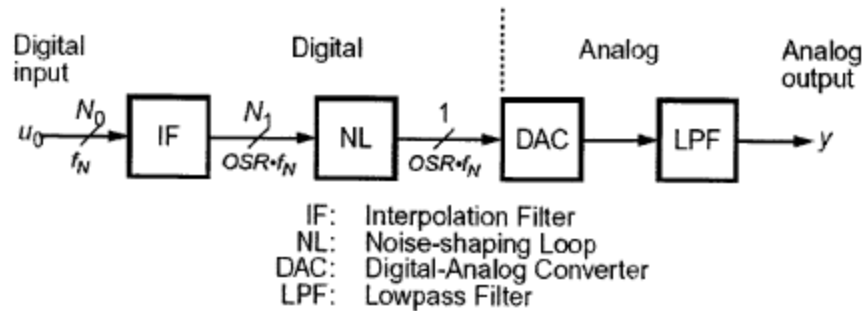
Block diagram of a ΔΣ DAC.

Single-bit DAC can be linear. For a few bits (2~4), DEM can be used
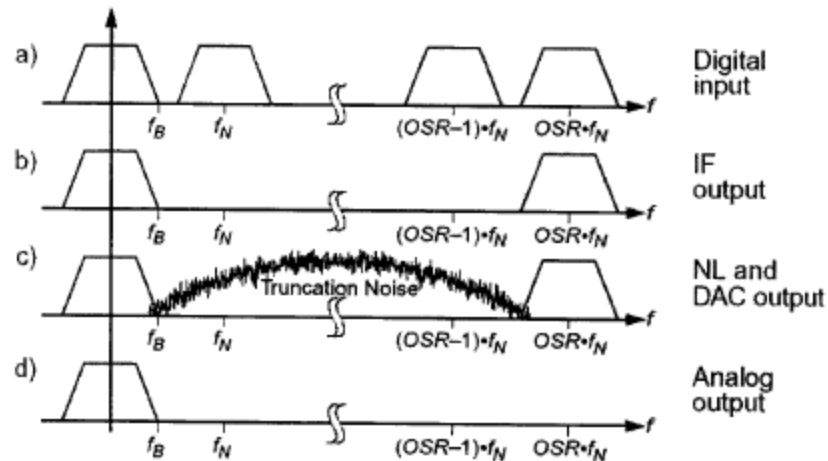
Signal and noise spectra in a ΔΣ DAC.

ΔΣ DAC Examples

Combined DAC, DCT and filter for a multi-bit ΔΣ DAC [8].

Another ΔΣ DAC with merged DAC, DCT and
SCF filter functions [15].
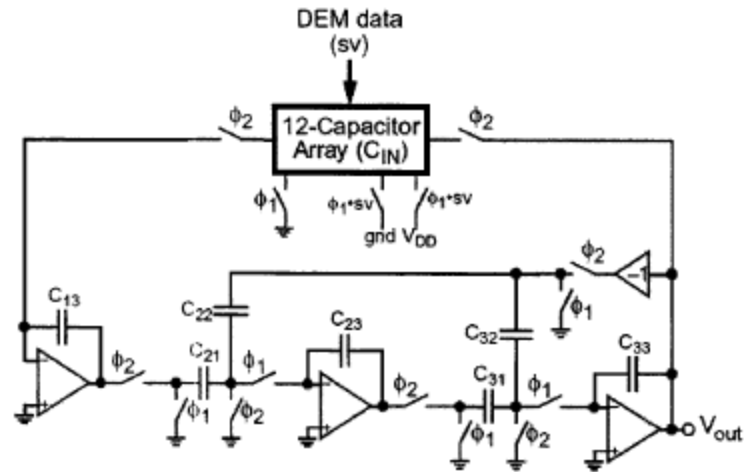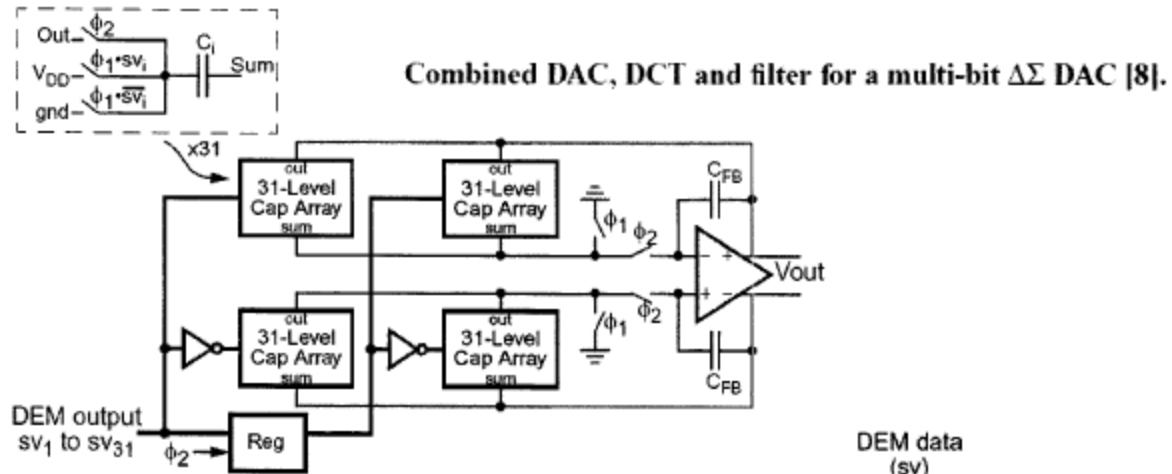
Micro-Power Delta-Sigma DACs

- Digital interpolation filter followed by digital D-S loop, and DCT stage performing D/A conversion and pre-filtering.

- Low-resolution SC DAC can be simple, low power.

- Easy trade-off between speed, accuracy and power dissipation.

- Passive R-C reconstruction filter may be possible.

$D_{in} \rightarrow$ [Interpolation Filter] $\rightarrow$ [$\Delta\Sigma$ Loop] $\rightarrow$ [SC DAC] $\rightarrow$ [Filter] $\rightarrow$ Vout
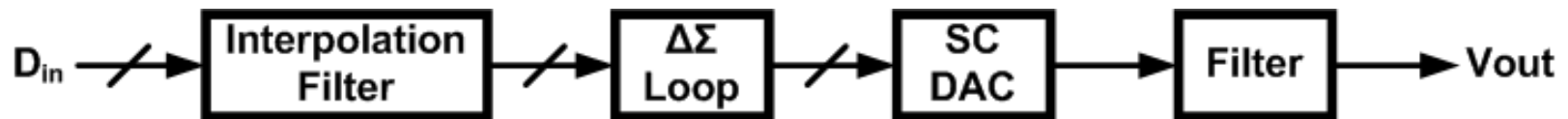
Classification of Nyquist-rate ADCs

(T=clock period, N=resolution in bits)

Algorithm	Conversion time	Latency (delay)	Resolution (typical)	Usual implementation
Parallel (flash)	T	T	5-9 bits	R string, comparators
Pipeline	T	NT	10-14 bits	SC stages+ T/H+ opamps.
Subranging (half-flash)	$2T$	$2T$	8-12 bits	R strings, comparators
Serial (Succ.appr)	NT	NT	7-12 bits	SC charge redistribution
Counting	$2^N T$	$2^N T$	16-24 bits	SC or CT integrator
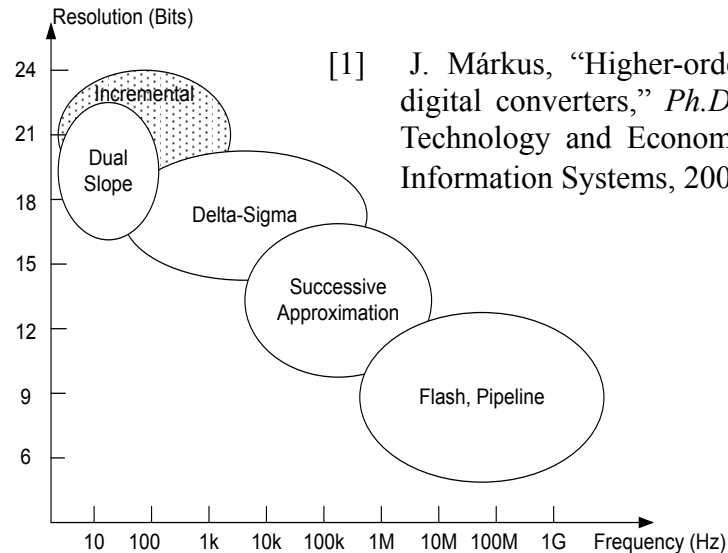
[1]   J. Márkus, "Higher-order incremental delta-sigma analog-to-digital converters," *Ph.D. dissertation*, Budapest University of Technology and Economics, Department of Measurement and Information Systems, 2005.

Successive-Approximation-Register ADC

- Serial operation: N cycles for N-bit resolution;
- DAC errors limit the accuracy;
- Needs S/H.
- For low speeds, the active blocks dissipate most power.

Various SAR ADCs [3],[4]

- The conventional SAR ADC
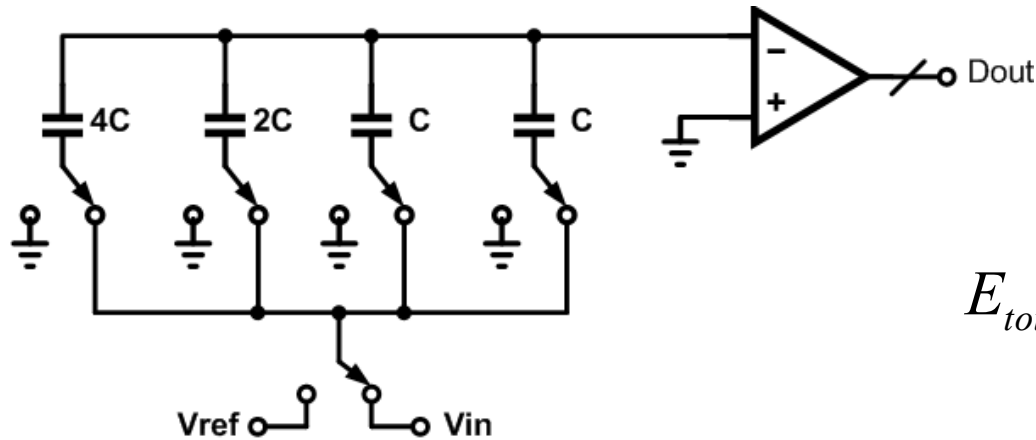
$$E_{total} = \frac{49}{8} CV_{ref}^2$$

- The junction-splitting SAR ADC
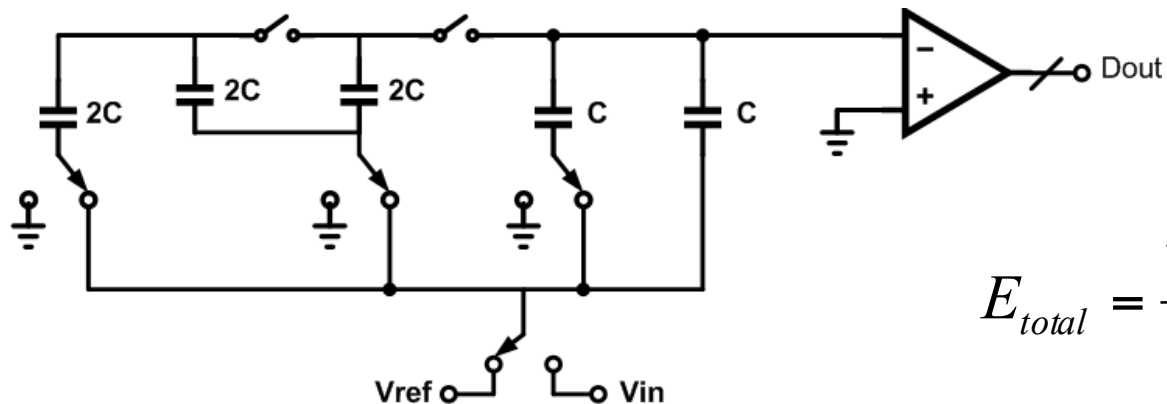
$$E_{total} = \frac{7}{8} CV_{ref}^2$$

Energy Loss in SAR C Arrays

Energy loss considerations:

- Energy required to charge an uncharged capacitor C to voltage V is $E = C.V^2$. Half is lost in the switch.

- In SAR ADC, for Vin = 0, the initial step draws an energy $2C.V_{ref}^2$ Joules, subsequent steps draw comparable amounts from V_{ref}.

- In the modified array, the first step draws $(C/2).V_{ref}^2$, the following ones less. The total energy is less than $C.V_{ref}^2$. Mismatch effects may be worse.

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Simpler SAR ADC Circuit

- Conventional implementation needs 2^N unit capacitors. Reduced cap implementation:
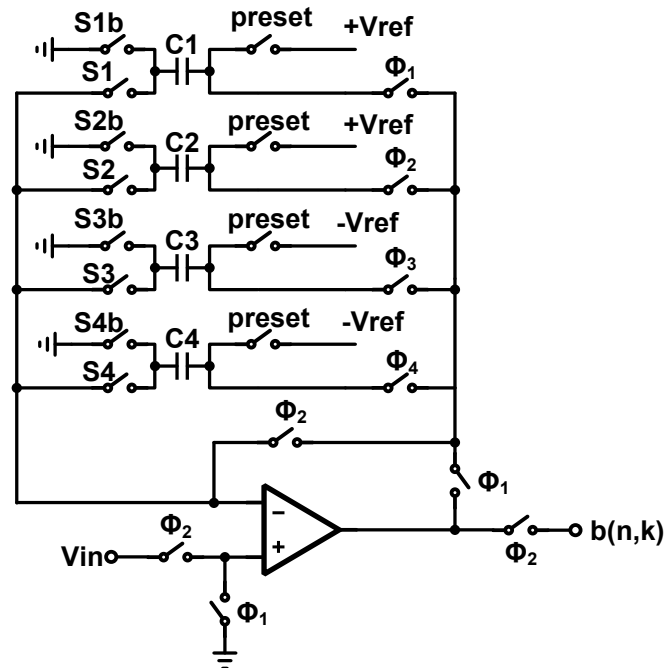
Needs 2N clock periods for every output word.

Simpler SAR ADC

- Four capacitors and a charge copier can generate all voltages for the SAR ADC.

- In each period, an upper limit, a lower limit and their average value are developed.

- The active block acts as a charge copier during $\Phi_1 = 1$, and as a comparator during $\Phi_2 = 1$.

- Active block needs more power than in other SAR ADCs.

Faster SAR ADC Circuit

- Faster implementation.
- Large spread of Cs and/or Vs.
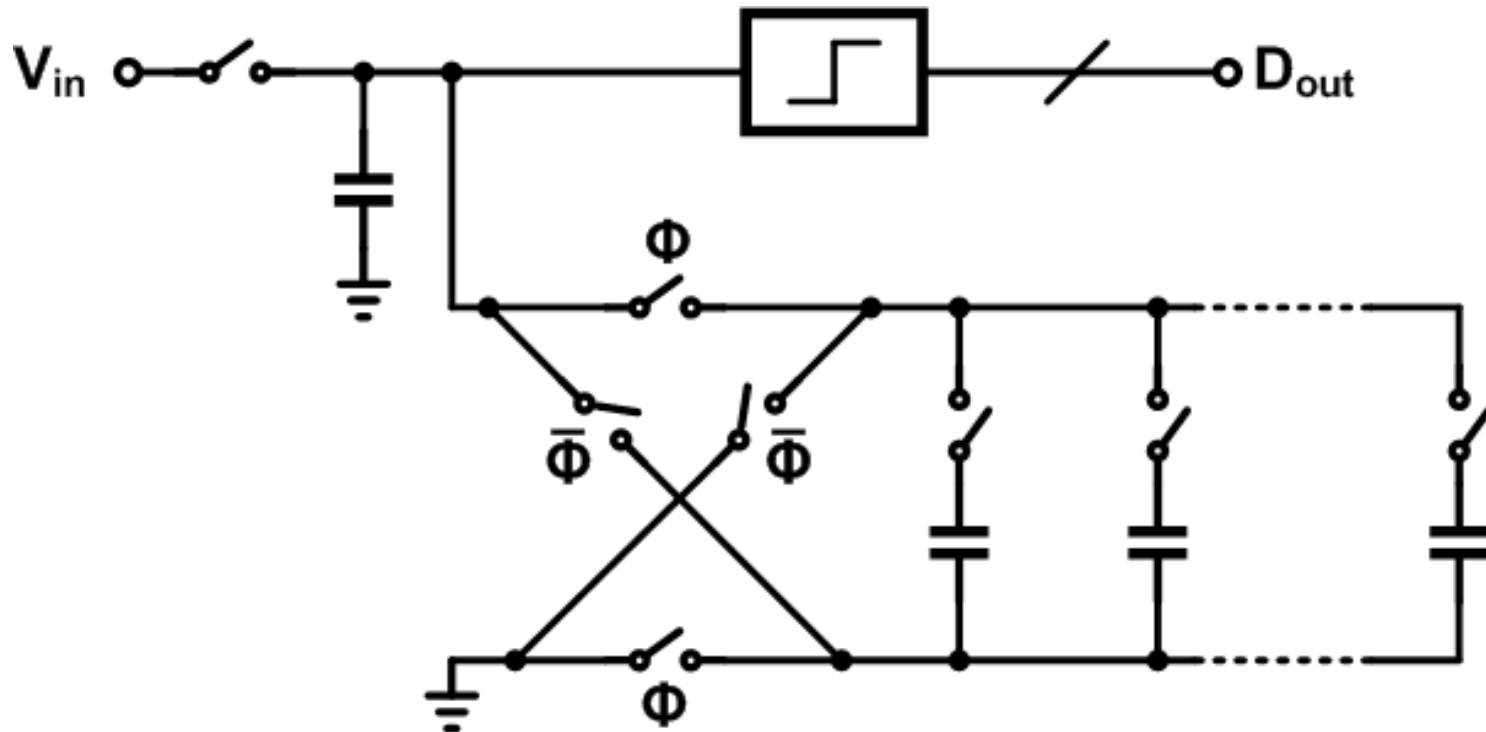
Faster SAR ADC

- Input capacitor is charged to V_{in}, and then the other capacitors add or subtract charges scaled from $C.V_r$ as controlled by the comparator output bits.

- The voltages are divided by 2 in each step.

- Also possible to use scaled capacitors and unscaled voltages, or scale both C and V.

- Concept shown only.

Junction-Splitting SAR

$$V_{out} = -V_{in} + \frac{C_T}{C_T + C_B} V_{ref}$$

Saves 75% average power compared to a conventional SAR ADC.
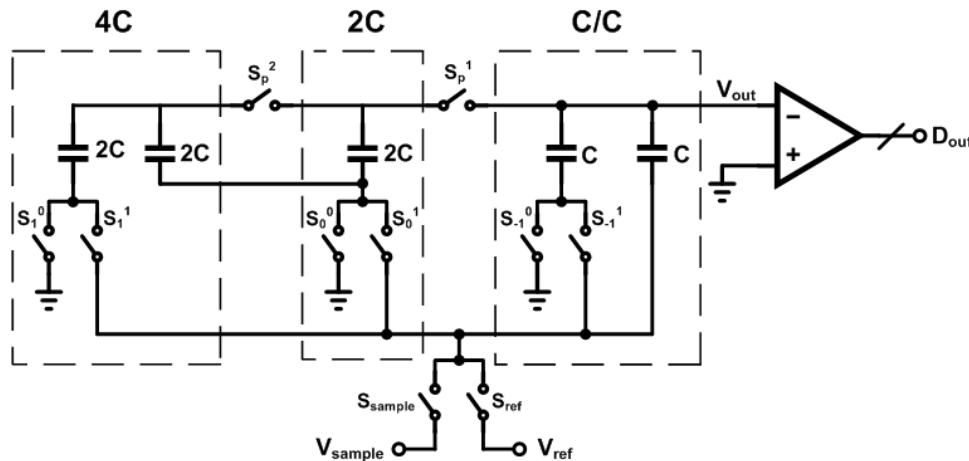
- A 3-bit junction-splitting SAR ADC.
- V_{out} is determined by the ratio of the capacitances, not by the absolute values.
- All blocks are appended to the capacitor array one-by-one, to generate the desired output voltage.
- Total capacitance: $2^N \cdot C$, where C is the unit capacitance.
- The power consumption for $V_{in}=0$ is

$$V_{ref}^2 \cdot C \cdot \left(1 - \frac{1}{2^N}\right)$$

* Lee, J.S., and Park, I.C.,: "Capacitor array structure and switch control for energy-efficient SAR analog-to-digital converters" , *ISCAS,* 2008, pp. 236-239

Pipeline SAR ADC

- Provides an output word each clock period – faster.
- Uses passive SC S/Hs and tapered DACs – low power.
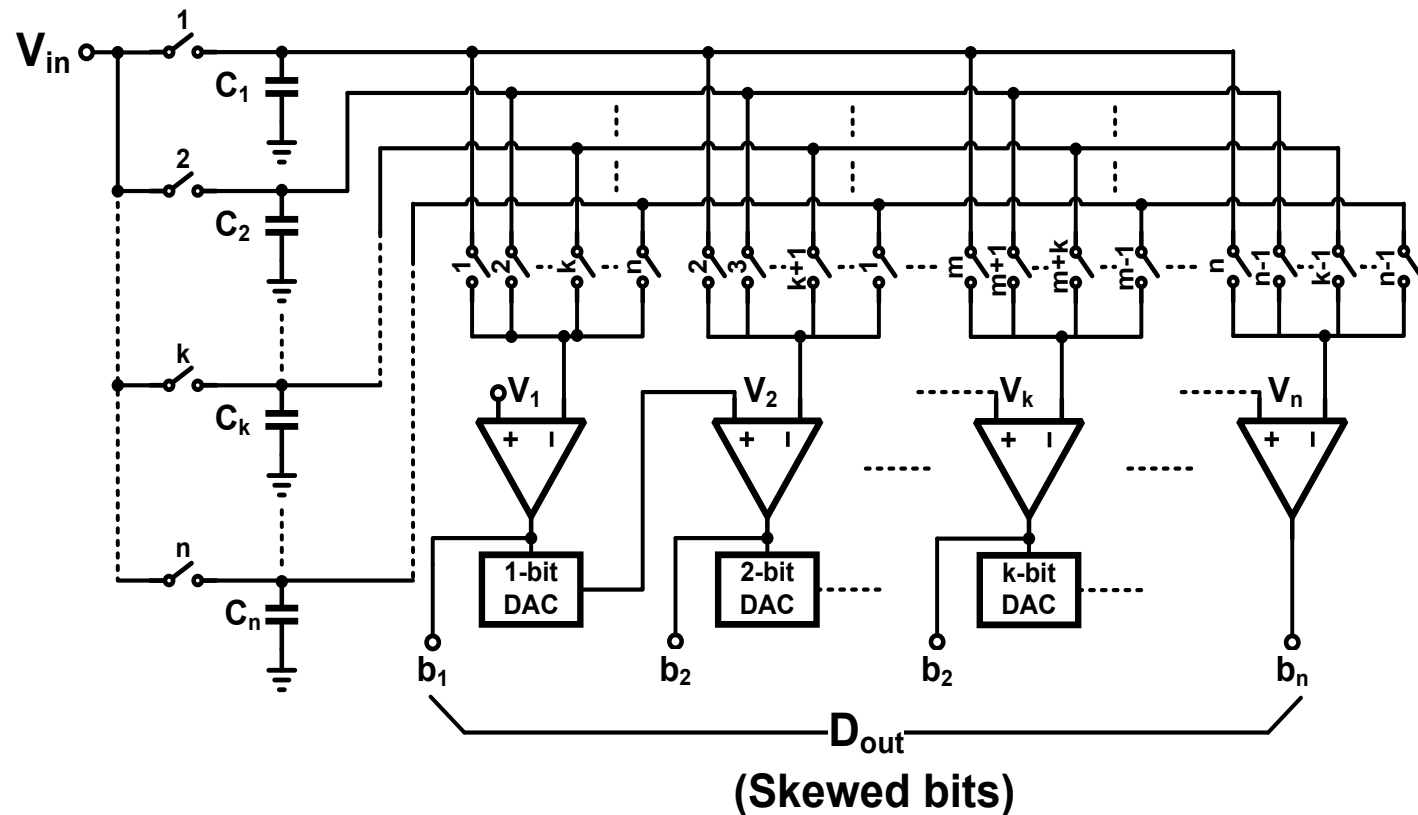
(Skewed bits)

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Using Junction-Splitting in Pipelined SAR ADC
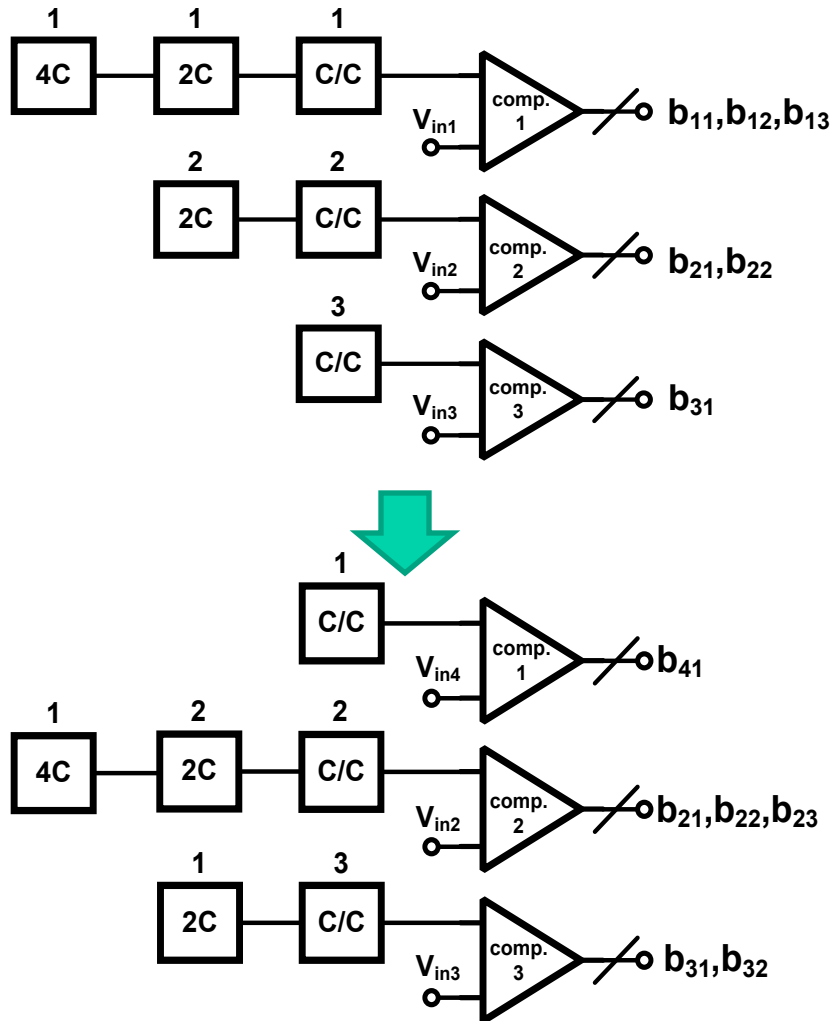
For 8-bit SAR ADC:

Conventional
256 C, 1X speed, 1X power consumption

Junction splitting
256 C, 1X speed, 0.25X power consumption

Junction-Splitting pipeline
512 C, 8X speed, 2X power consumption

* J. Lin, W. Yu and G. C. Temes, "Micro-power time-interleaved and pipelined SAR ADCs," ISCAS 2010

Two-Step Split-Junction SAR ADC
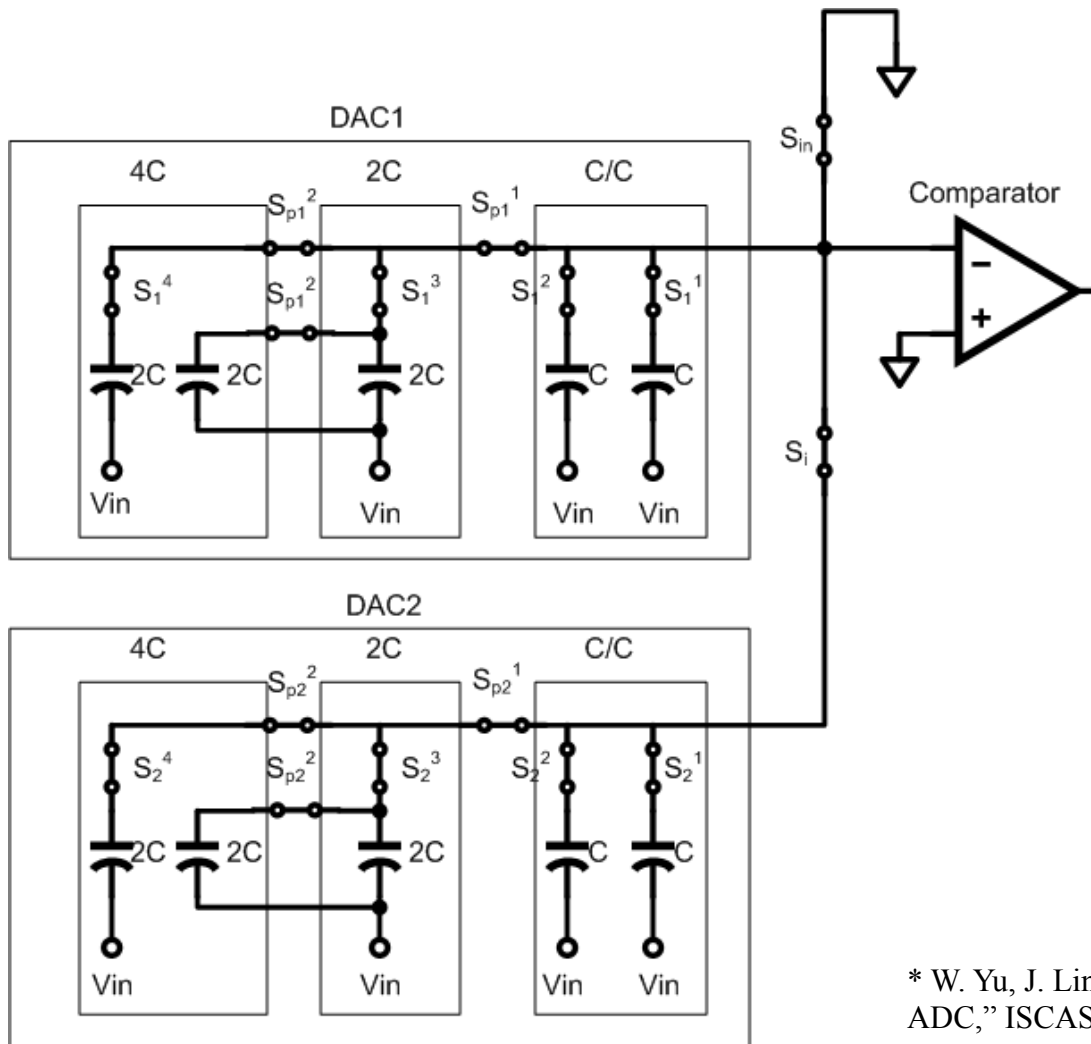
e.g. 6-bit SAR

first 3 bits (MSB)

coarse quantization, the same as split-junction SAR

last 3 bits (LSB)

fine quantization, interpolate with DAC1 and DAC2

Save 8X capacitor area and power consumption.

* W. Yu, J. Lin and G. C. Temes, "Two-Step Split-Junction SAR ADC," ISCAS 2010

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Power Consumption vs. Output Digital Code

Comparison of Different SAR ADCs

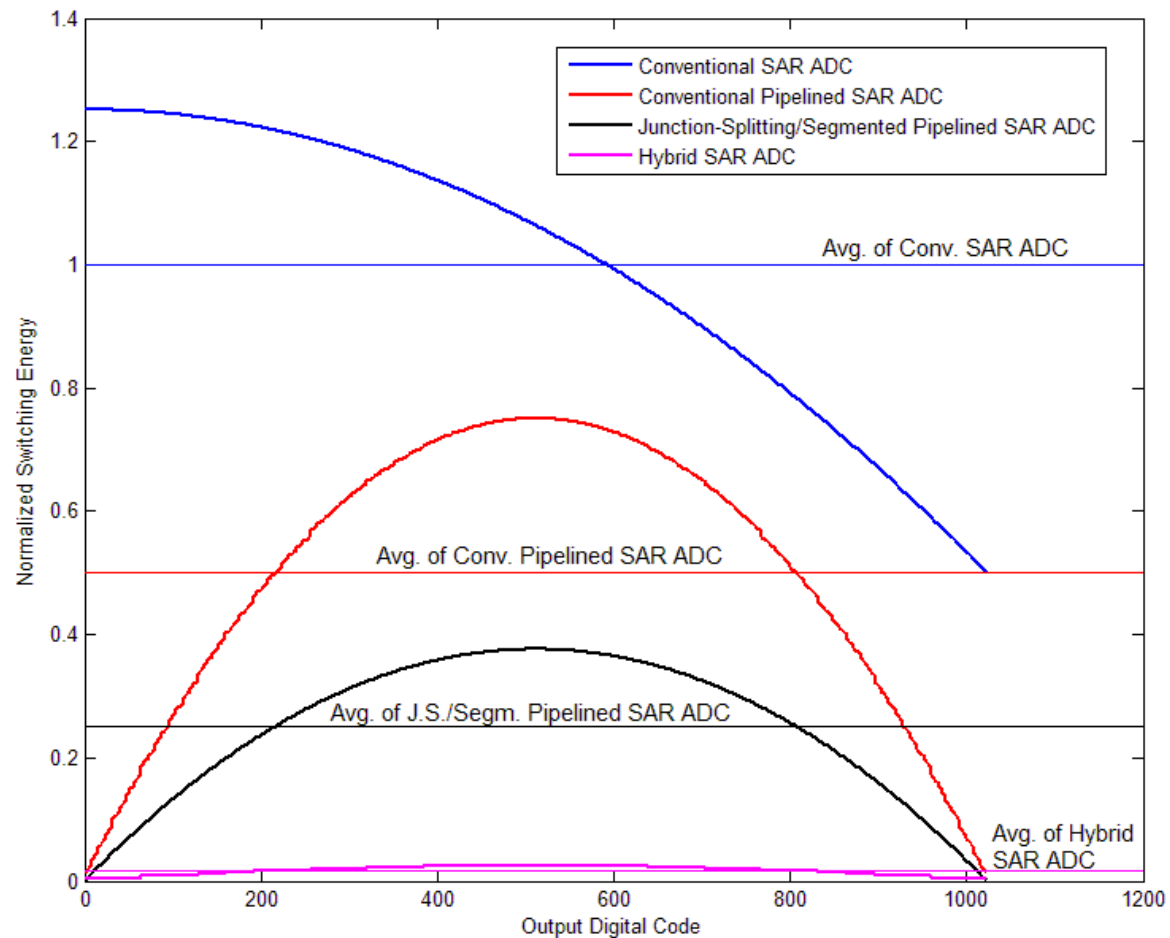| Configuration	Throughput (word/period)	$P_{Dynamic}/CV_{ref}^2$ for code $00\cdots0$	Total Capacitance	Number of Switches
Conv. Single SAR ADC	1/N	$\frac{5}{6}\cdot 2^N - \frac{1}{2}\cdot 2^{-N} - 1$	$2^N\cdot C$	$2\cdot(N+1)$
Energy-efficient Single SAR ADC	1/N	$1-2^{-N}$	$2^N\cdot C$	$3\cdot N-1$
Conv. T.I. SAR ADC	1	$\frac{5}{6}\cdot 2^N - \frac{1}{2}\cdot 2^{-N} - 1$	$N\cdot 2^N\cdot C$	$2\cdot N\cdot(N+1)$
T.I. Segmented SAR ADC	1	$1-2^{-N}$	$(2^{N+1}-2)\cdot C$	$\frac{1}{3}N^3 + N^2 + \frac{2}{3}N$
Conv. Pipelined SAR ADC	1	$N-1+2^{-N}$	$(2^{N+1}-2)\cdot C$	$\frac{1}{2}N^2 + \frac{1}{2}N - 1$
Segmented Pipelined SAR ADC	1	$1-2^{-N}$	$(2^{N+1}-2)\cdot C$	$\frac{1}{3}N^3 + 2N^2 + \frac{2}{3}N$
Hybrid SAR ADC	1/(N+1)	$1-2^{-\frac{N}{2}}$ N is an even.	$2^{\frac{N}{2}+1}\cdot C$ N is an even.	$\frac{1}{4}N^2 + \frac{7}{2}N + 1$ N is an even.
		$1-2^{-\frac{N+1}{2}}$ N is an odd.	$2^{\frac{N+1}{2}+1}\cdot C$ N is an odd.	$\frac{1}{4}N^2 + 4N + \frac{19}{4}$ N is an odd.

ADC Architectures
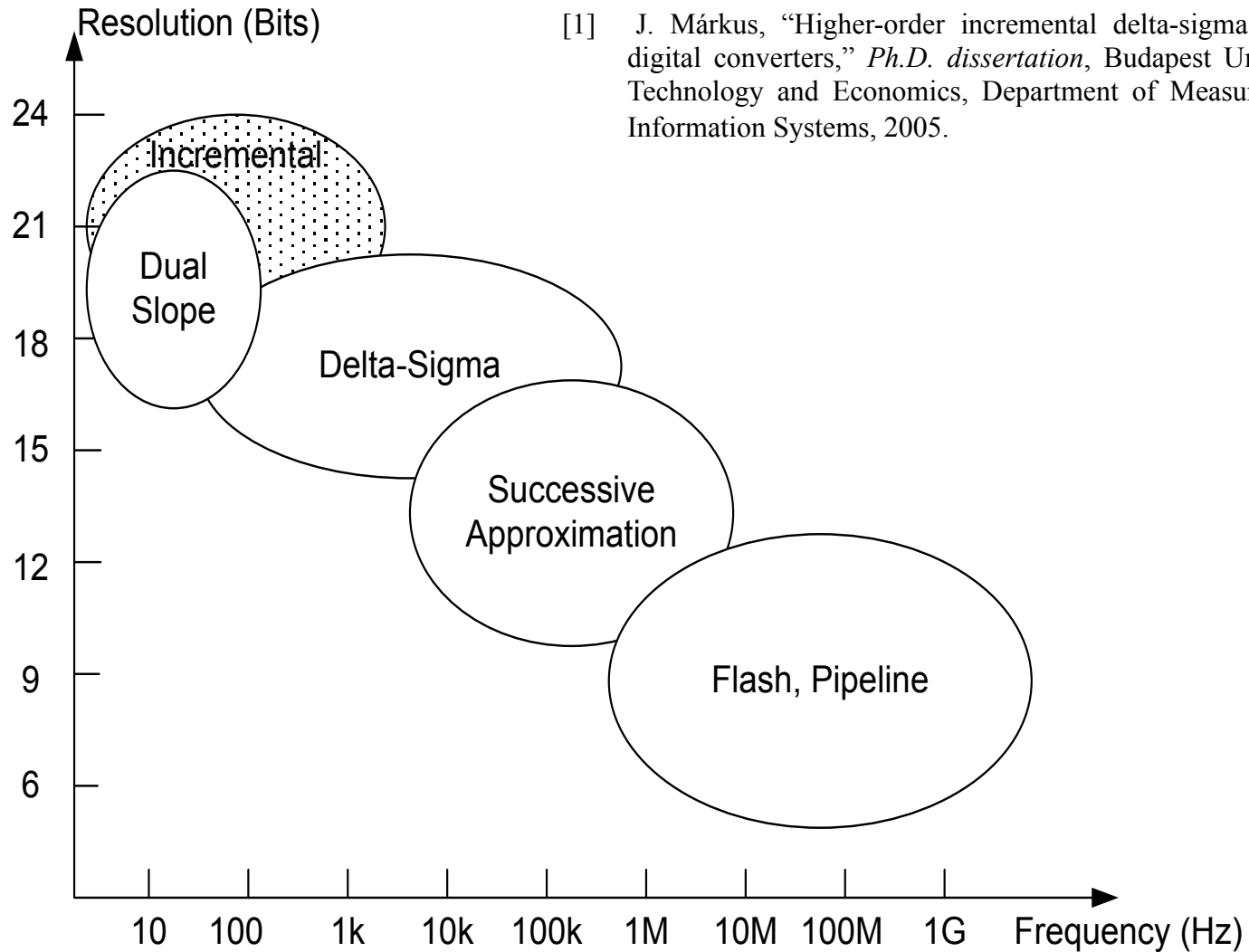
Resolution (Bits)

[1] J. Márkus, "Higher-order incremental delta-sigma analog-to-digital converters," *Ph.D. dissertation*, Budapest University of Technology and Economics, Department of Measurement and Information Systems, 2005.

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Delta-Sigma (ΔΣ) Modulators
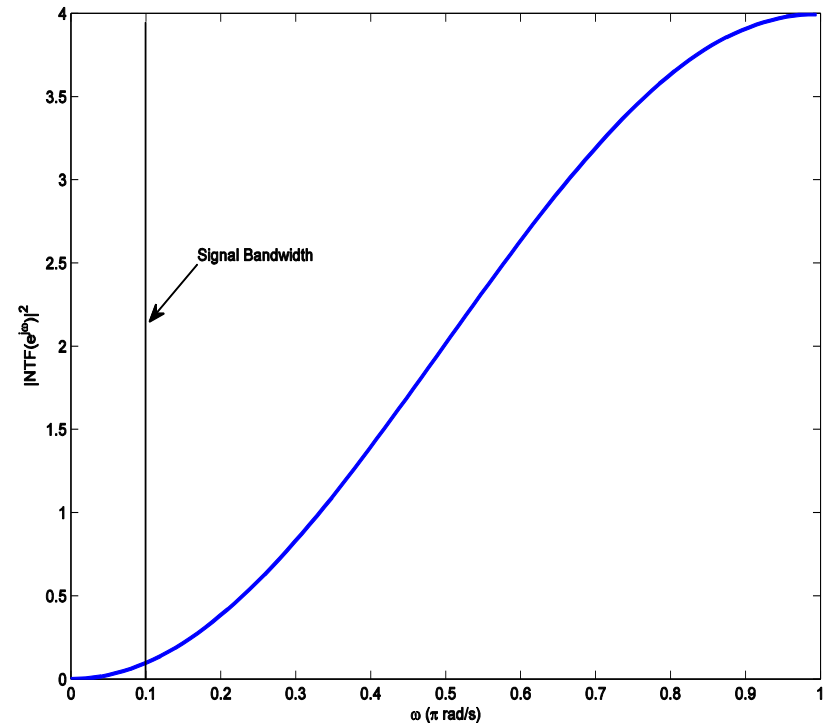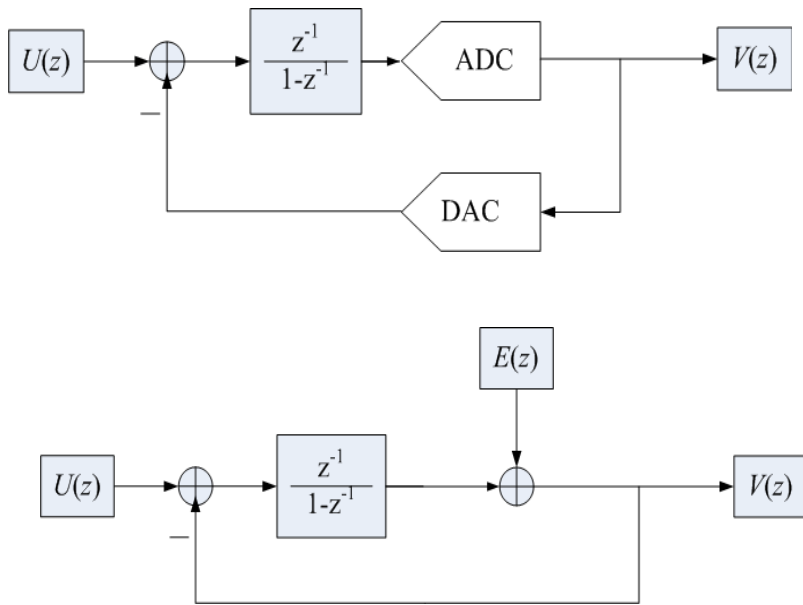
[2]   R. Schreier and G. C. Temes, *Understanding Delta-Sigma Data Converters*, Piscataway, NJ: IEEE Press/ Wiley, 2005.

$$STF(z) = z^{-1}$$

$$NTF(z) = 1 - z^{-1}$$

Incremental ADC
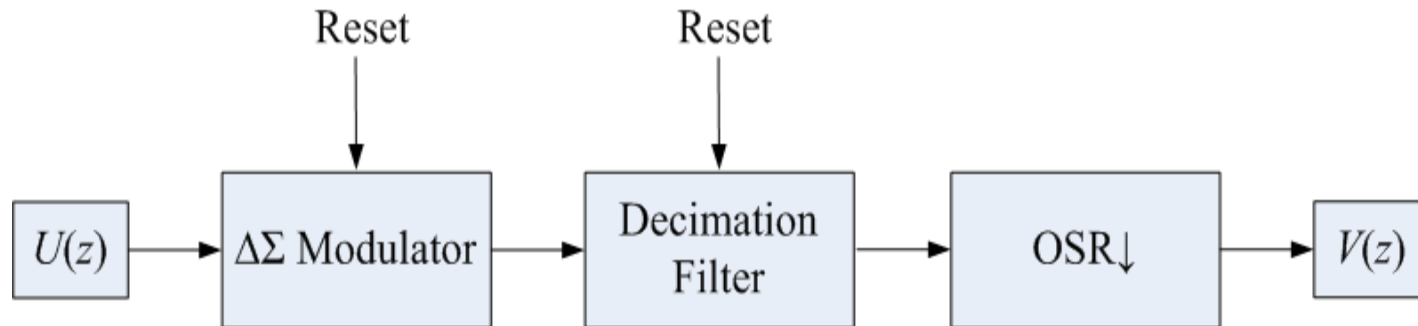
Incremental ADCs: $\Delta\Sigma$ ADCs which are reset after each conversion.
Properties:

• Flexible trade-off between OSR and power dissipation;

• Limited memory – stable and not tonal;

• Well suited for instrumentation and measurement (I&M) applications;

• High absolute accuracy possible;

• Allows for accurate gain and offset error correction;

• Easily multiplexed, or operated intermittently.

Incremental ADC - Publications

- **First incremental ADC (bipolar, 17-bit resolution, first-order $\Delta\Sigma$ loop)**

- R. J. Plassche, "A sigma-delta modulator as an A/D converter," *IEEE Trans. on Circuits and Systems*, vol. 25, no. 7, pp. 510–514, 1978.

- **Further research (CMOS, 16-bit resolution, first-order $\Delta\Sigma$ loop)**

- J. Robert, G. C. Temes, V. Valencic, R. Dessoulavy and P. Deval, "A 16-bit low-voltage A/D converter," *IEEE Journal of Solid-State Circuits*, vol. 22, no. 2, pp. 157–163, 1987.

- **Multi-Stage Noise Shaping (MASH) incremental ADC (two first-order $\Delta\Sigma$ loops)**

- J. Robert and P. Deval, "A second-order high-resolution incremental A/D converter with offset and charge injection compensation," *IEEE Journal of Solid-State Circuits*, vol. 23, no. 3, pp. 736–741, 1988.

- **22-bit incremental ADC (third-order $\Delta\Sigma$ loops, 0.3 mW power consumption)**

- V. Quiquempoix, P. Deval, A. Barreto, G. Bellini, J. Márkus, J. Silva and G. C. Temes, "A low-power 22-bit incremental ADC," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 7, pp. 1562–71, 2006.

- **Wideband applications (low OSR, 7th-order MASH)**

- T. C. Caldwell and D. A. Johns, "An incremental data converter with an oversampling ratio of 3," *PhD Research in Microelectronics and Electronics Conference (PRIME)*, 2006, pp. 125–128.

Incremental ADC – Commercial Chips

Sometimes referred to as charge-balancing $\Delta\Sigma$ ADCs, one-shot $\Delta\Sigma$ ADCs or no-latency $\Delta\Sigma$ ADCs.

- **AD77xx product family, Analog Devices**
  16-bit ~ 24-bit resolution, 1~10 channels, 60~2.5M SPS

- **ADS124x product family, Burr-Brown (Texas Instruments)**
  24-bit resolution, 4~8 channels, 15 SPS

- **CS55xx product family, Cirrus Logic**
  24-bit resolution, 6.25~3840 SPS

- **LTC24xx product family, Linear Technology**
  16-bit ~ 24-bit resolution, 1~16 channels, 6.9~8000 SPS

Second-Order Incremental ADC
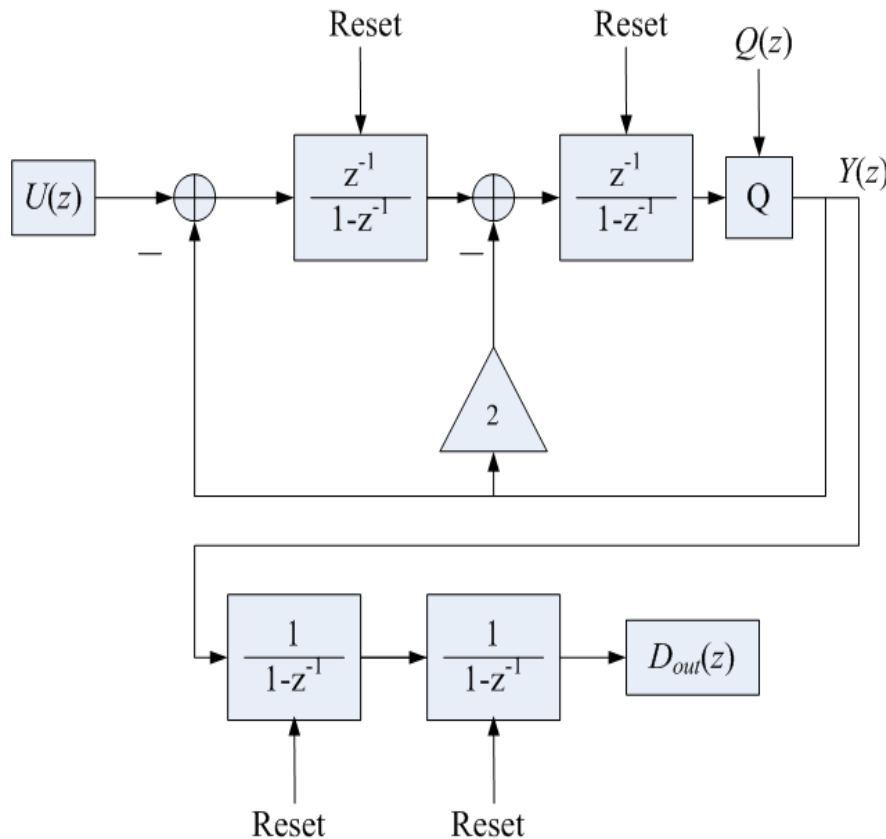
$$Y(z) = z^{-2}U(z) + (1 - z^{-1})^2 Q(z)$$

$$D_{out}(z) = Y(z) \frac{1}{(1 - z^{-1})^2} = \frac{z^{-2}}{(1 - z^{-1})^2} U(z) + Q(z)$$

$$d_{out} = \frac{M(M - 1)}{2} u + q(M)$$

$$D = 2d_{out} / M(M - 1)$$

$$|\varepsilon| = |D - u| = \left| \frac{2q(M)}{M(M - 1)} \right| \leq \frac{2V_{ref}}{(l - 1)M(M - 1)}$$

Conversion time: $M = \dfrac{\sqrt{2} \cdot 2^{n/2}}{\sqrt{l - 1}}$ clock periods;

l: number of quantizer levels.

[1]   J. Márkus, "Higher-order incremental delta-sigma analog-to-digital converters," *Ph.D. dissertation*, Budapest University of Technology and Economics, Department of Measurement and Information Systems, 2005.

Low-Distortion Third-Order Structure (1)

$$\left|v_3(k)\right| \le V_{ref}$$
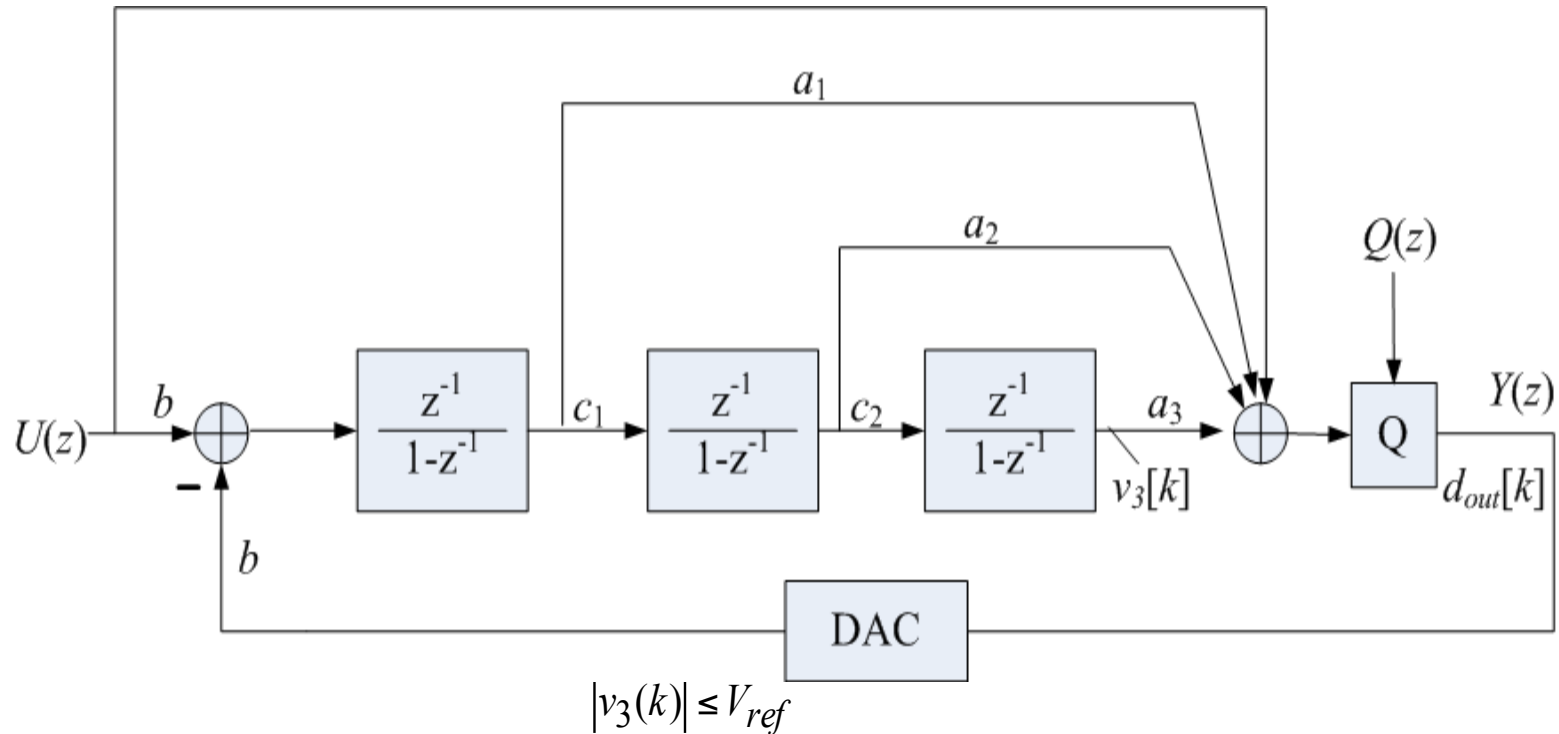
$$Y(z) = U(z) + (1 - z^{-1})^L Q(z)$$

$$U(z) - Y(z) = -(1 - z^{-1})^L Q(z)$$

Only quantization noise $Q(z)$ propagates through the integrators.

[3]   J. Silva, U.-K. Moon and G. C. Temes, "Low-distortion delta-sigma topologies for MASH architectures", *Proc. of the International Symposium on Circuits and Systems*, vol. 1, pp. 1144–1147, 2004.

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Low-Distortion Third-Order Structure (2)

$$\left| u - \frac{3 \cdot 2}{M(M-1)(M-2)} \sum_{m=0}^{M-1} \sum_{l=0}^{m-1} \sum_{k=0}^{l-1} d_{out}[k]V_{ref} \right| \leq \frac{3 \cdot 2 \cdot V_{ref}}{bc_1c_2M(M-1)(M-2)}$$

$$D = \frac{3 \cdot 2}{M(M-1)(M-2)} \sum_{m=0}^{M-1} \sum_{l=0}^{m-1} \sum_{k=0}^{l-1} d_{out}[k]V_{ref}$$

$$\left| \varepsilon \right| = \left| u - D \right| \leq \frac{3 \cdot 2 \cdot V_{ref}}{bc_1c_2M(M-1)(M-2)}$$

[1]   J. Márkus, "Higher-order incremental delta-sigma analog-to-digital converters," *Ph.D. dissertation*, Budapest University of Technology and Economics, Department of Measurement and Information Systems, 2005.
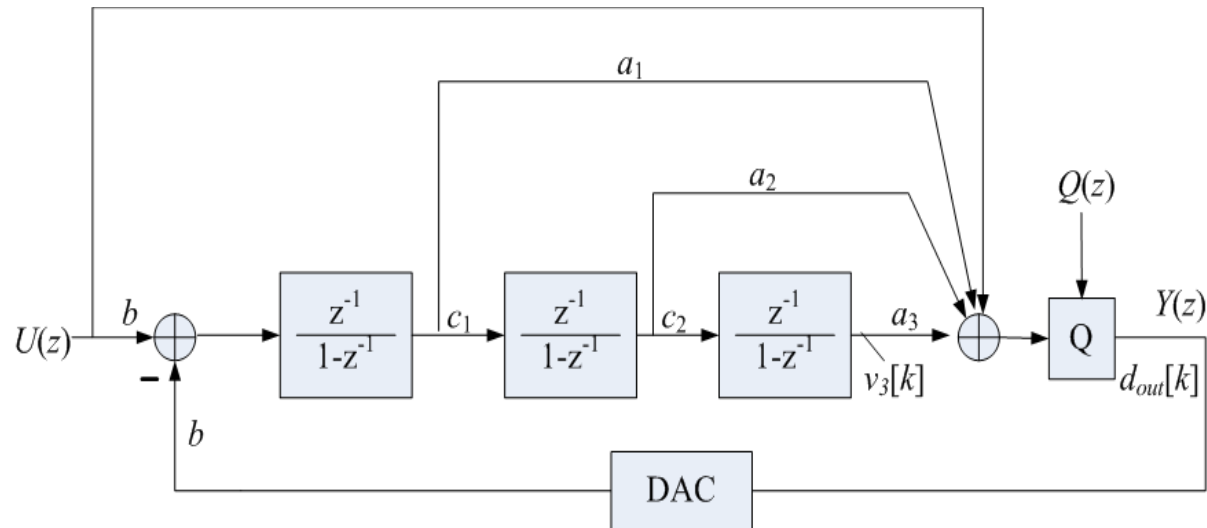
Offset Correction in Integrators (1)
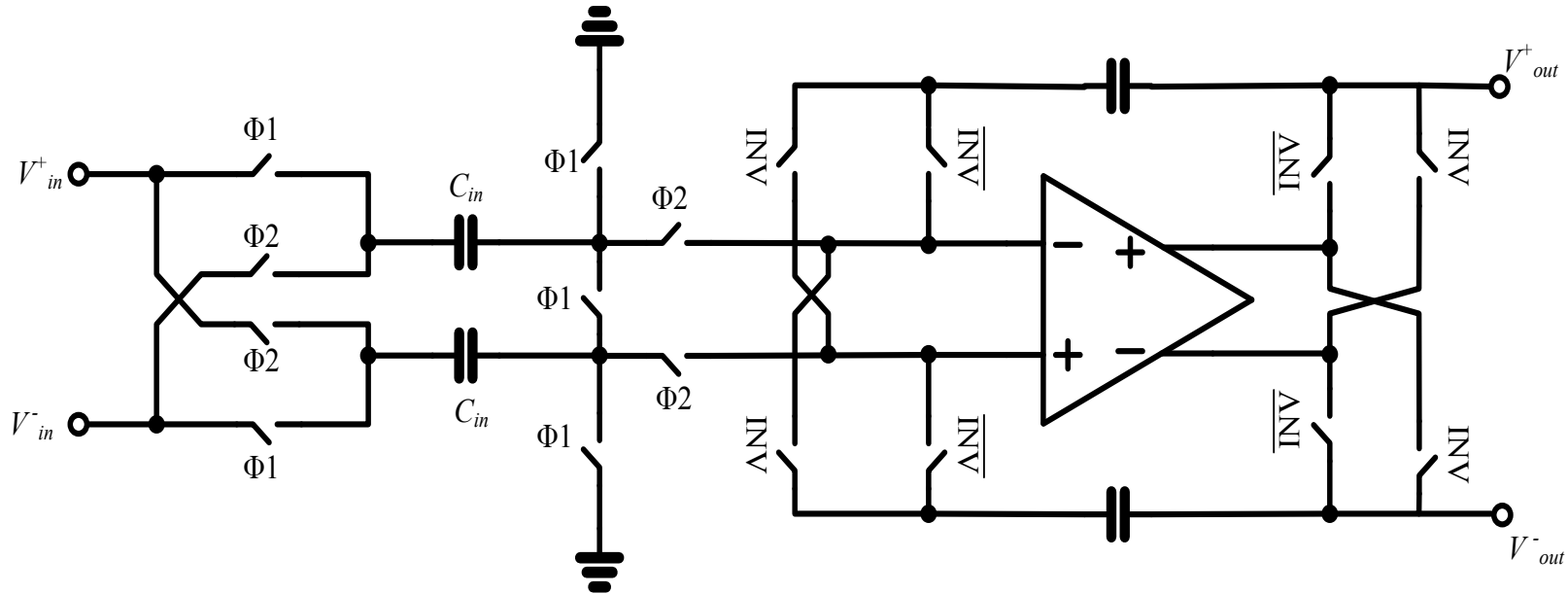
[4]   V. Quiquempoix, P. Deval, A. Barreto, G. Bellini, J. Márkus, J. Silva and G. C. Temes, "A low-power 22-bit incremental ADC," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 7, pp. 1562–71, 2006.

Offset Correction in Integrators (2)

Generalization of chopper stabilization.

Changing the first opamp polarity according to fractal sequencing

$$S_1 = (+ \ -)$$

$$S_2 = (S_1 \bar{S_1}) = ((+ \ -)(- \ +))$$

$$...$$

$$S_n = (S_{n-1} \bar{S}_{n-1})$$

If S_n is used for n-th order modulator, and the modulator runs for M clock periods, where $M/2^n$ is an integer, the opamp offset will be cancelled.

[4] V. Quiquempoix, P. Deval, A. Barreto, G. Bellini, J. Márkus, J. Silva and G. C. Temes, "A low-power 22-bit incremental ADC," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 7, pp. 1562–71, 2006.

Multiplexed Incremental ADC

ADC shared between N channels
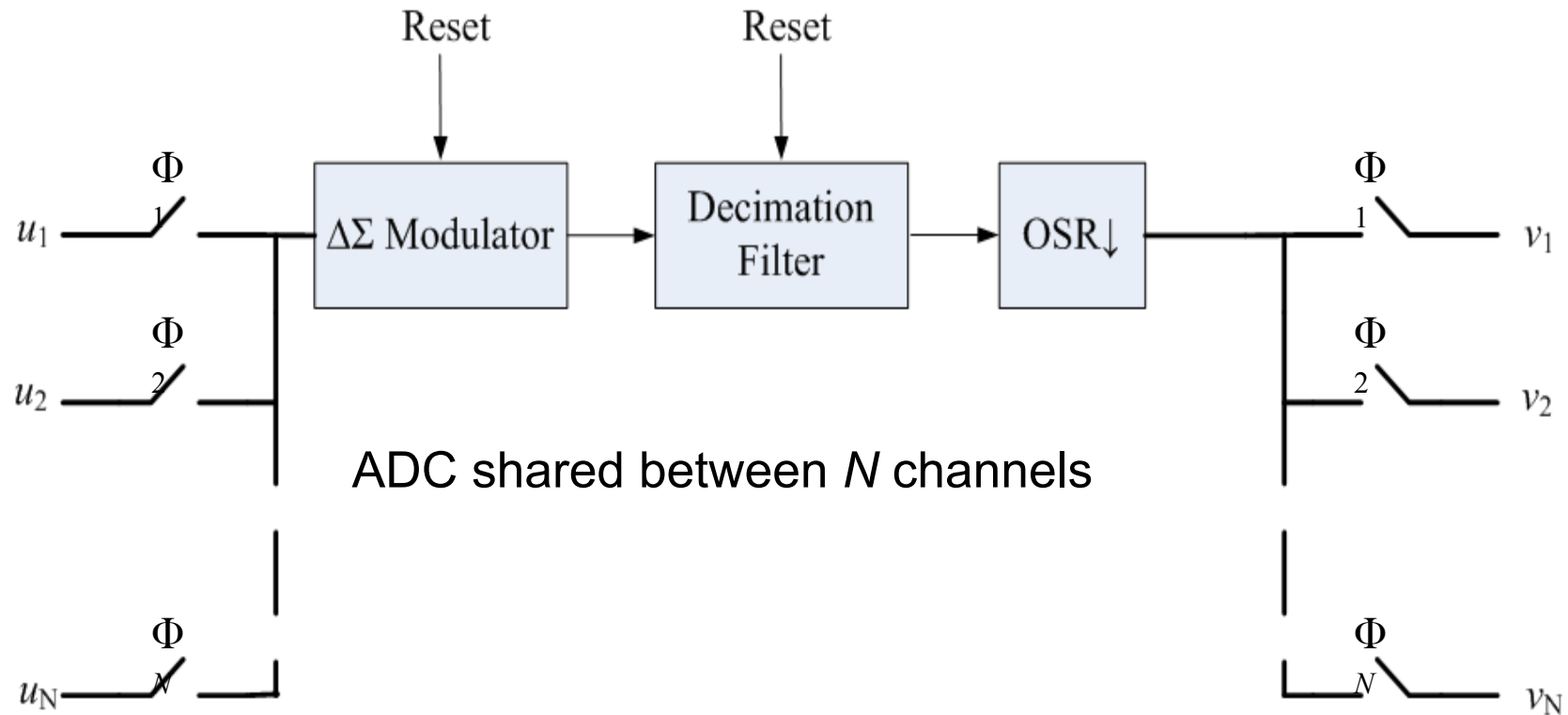
Analysis of Incremental ADC

$$v(n) = \left[stf\,'(k) * u(k) + stf\,'(k) * t(k) + ntf\,'(k) * q(k) \right]_{M,n}$$

$v(n)$ is the single output value obtained in the nth conversion cycle

$u(k)$ is the input signal

$t(k)$ is the input-referred thermal noise

$q(k)$ is the quantization noise

$stf'(k)$ is the impulse response of the overall signal transfer function $STF(z)H(z)$

$ntf'(k)$ is the impulse response of the overall noise transfer function $NTF(z)H(z)$

$H(z)$ is the transfer function of the decimation filter

Both $stf'(k)$ and $ntf'(k)$ have finite lengths (length=M)

M is the number of clock periods in each conversion cycle

[5] J. Steensgaard, Z. Zhang, W. Yu, A. Sárhegyi, L. Lucchese, D.-I. Kim and G. C. Temes, "Noise-power optimization of incremental data converters," to appear in *IEEE Transactions on Circuits and Systems I*, 2008.

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Noise Optimization in Incremental ADC

To minimize the overall output noise power

$$\min_{\mathbf{h}} \overline{v_n^2} = \mathbf{h}^T \cdot \mathbf{O} \cdot \mathbf{h},$$

where

$$\mathbf{O} = \frac{5kT}{C_{in}} \mathbf{S}^T \mathbf{S} + \frac{\Delta^2}{6} \mathbf{N}^T \mathbf{N}$$

S and N are matrices constructed from the *stf*(*k*) and *ntf*(*k*) sequences.

The problem can be formulated as quadratic programming, or solved analytically for the optimum *h*(*n*).

The digital filter is FIR; can be realized as a single multiply-accumulate block.

[5]   J. Steensgaard, Z. Zhang, W. Yu, A. Sárhegyi, L. Lucchese, D.-I. Kim and G. C. Temes, "Noise-power optimization of incremental data converters," to appear in *IEEE Transactions on Circuits and Systems I*, 2008.

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ADC with Extended Range
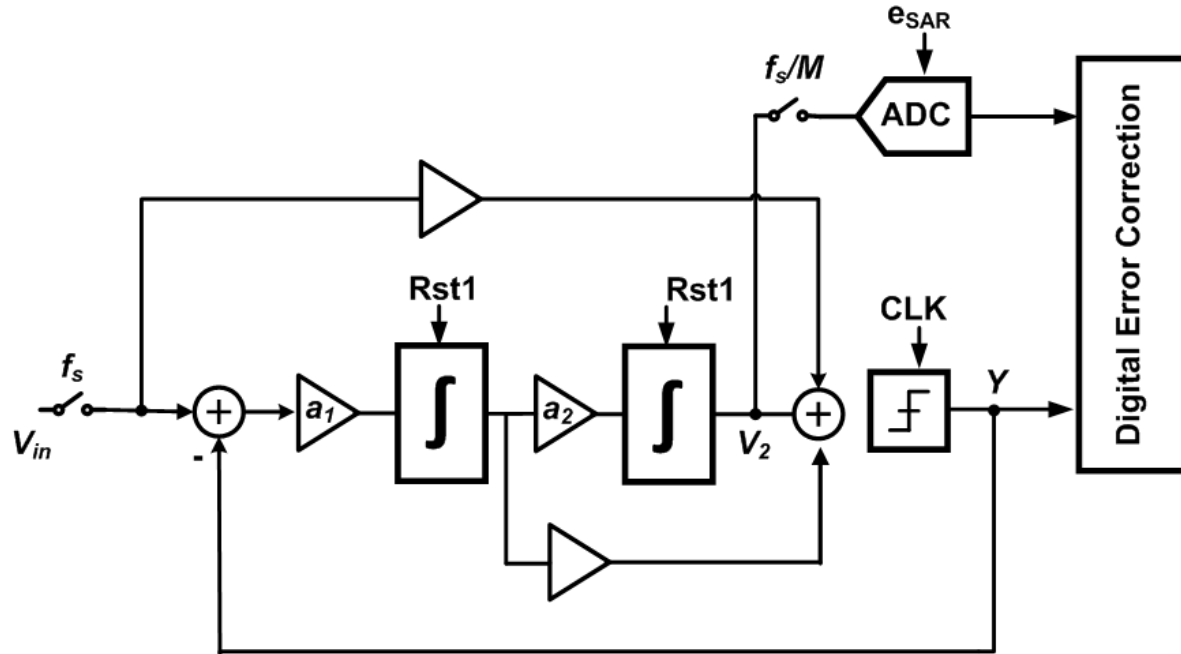
- **Features of Extended-Range ADC:**

1. Incremental $\Delta\Sigma$ modulator operates at oversampled frequency f_s.

2. Feedforward topology is used to lower the signal swings.

3. The 2nd stage ADC converts the residual error at the 1st stage output.

4. The 2nd stage may use a SAR ADC, with an operating frequency f_s/M.

Operation of Extended-Counting ADC
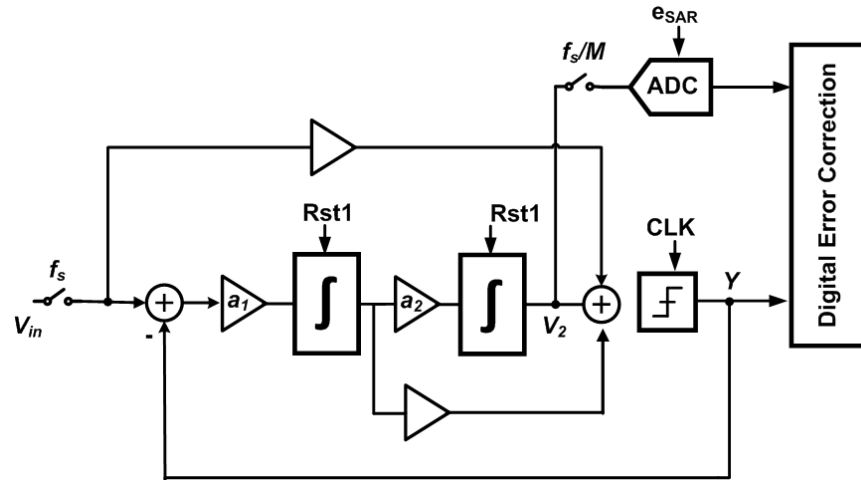
- After M cycles, $v_2(M)$ becomes

$$v_2(M) = a_1 \cdot a_2 \cdot \frac{M(M-1)}{2} \cdot v_{in} + a_1 \cdot a_2 \cdot V_{ref} \cdot \sum_{j=1}^{M} (M-j) \cdot Y(j)$$

- $v_2(M)$ is converted by the 2nd ADC and combined with the triangularly-weighted output sequence.

- The overall quantization error is ideally only the quantization error of the SAR ADC:

$$E_{Q-ADC} = \frac{2}{a_1 \cdot a_2 \cdot M \cdot (M-1)} E_{Q-SAR}$$

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Circuit Implementation

SAR ADC
- 11-bit resolution
- dual-capacitor array to reduce the total input capacitance to 3pF, using a unit cap 48fF
- Conversion in 11 cycles of charge redistribution.

Incremental ΔΣ Modulator
- Clock frequency = 45.2MHz.
- OSR = 45.

Measured Spectrum
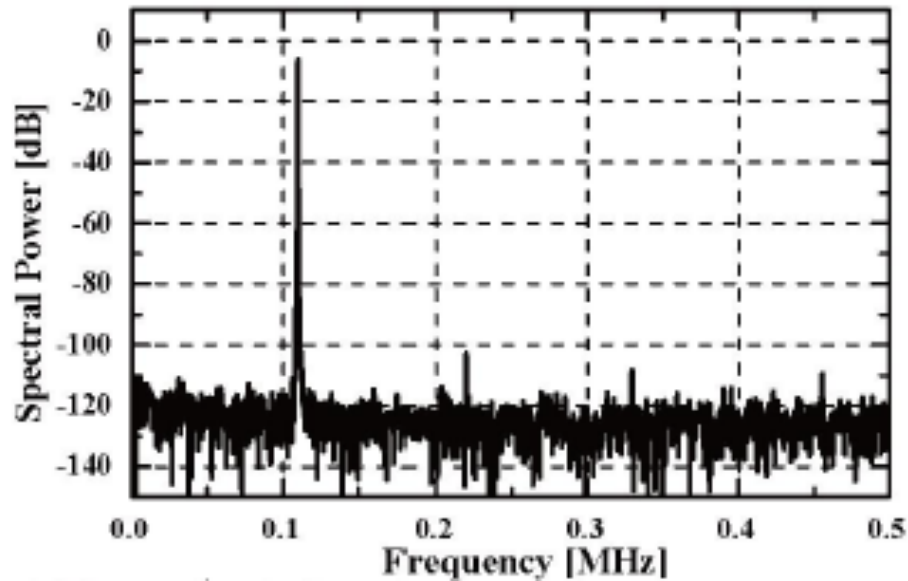
Measured Results
- Signal: -6dB, 110kHz
- peak SNDR is 86.3 dB, SFDR is 97 dB
- ADC achieved 90.1dB dynamic range.
- 38mW power dissipation (excluding output drivers), out of which 23mW is consumed in the 1st opamp, 9mW in the 2nd opamp, 1mW in the SAR, less than 5mW in all of the digital blocks

References on DACs

References

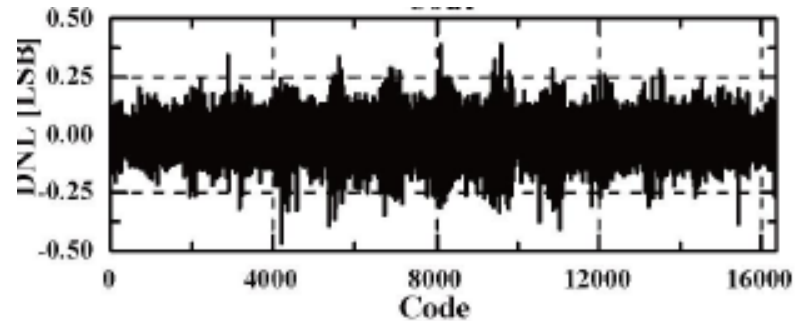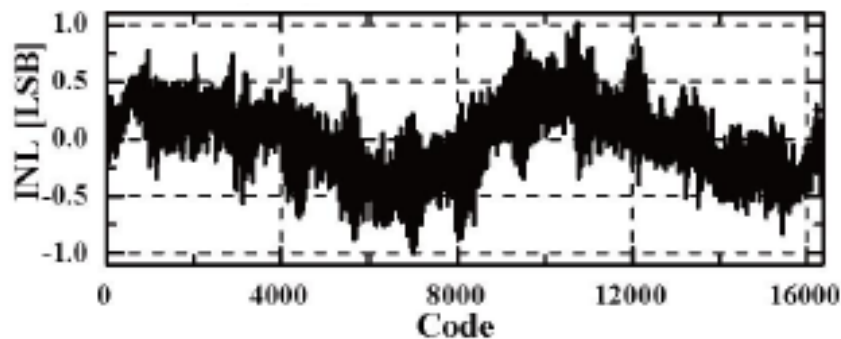[1]   P. J. Naus, E. C. Dijkmans, E. F. Stikvoort, A. J. McKnight, D. J. Holland, and W. Brandinal., "A CMOS stereo 16-bit D/A converter for digital audio," *IEEE Journal of Solid-State Circuits*, vol. 22, pp. 390-395, June 1987

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[9]   D. Groeneveld et al., "A self-calibration technique for monolithic high-resolution D/A converters," IEEE J. Solid-State Circuits, vol. 24, pp. 1517-1522, Dec. 1989.

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[15] M. Annovazzi et al., "A low-power 98-dB multibit audio DAC in a standard 3.3-V 0.35-μm CMOS technology," *IEEE Journal of Solid-State Circuits*, vol. 37, pp. 825-834, July 2002.

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